MAINTENANCE MANUAL
SYSTEM MODULE 19D902590G1-G3

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DESCRIPTION

System Module 19D902590 contains all audio processing and control circuitry for the T/R Shelf. The audio processing and routing is done using analog circuitry. The control circuitry utilizes high speed digital components, and includes a microprocessor.

System Module 19D902590G3 is a 19D902590G1 System Module with a "piggyback" Digital Signal Processor (DSP) board (19D902667G1). Due to the high speed digital circuitry, the System Module is housed in an RFI and EMI shield.

Supply voltages for the System Module and DSP board are generated by the Power Module and applied to the System Module through the backplane. All audio and control signals are routed to the System Module through the 96-pin DIN connectors on the backplane board.

CIRCUIT ANALYSIS

SYSTEM BOARD

Clock Circuitry

The 14.7456MHz clock drive for the System Module's digital circuitry is derived from a gate oscillator circuit comprised of U21C, U21D, Y1 and associated components. R110 keeps the inverter gate U21C in the linear mode during power-up for reliable clock start-up. R111 and C3 provide AC and DC drive to crystal Y1. U21D buffers the clock signal, and Q11 and Q12 are provided to allow the microprocessor (U1) to adjust the clock frequency.

When the microprocessor pulls P4.5 (pin 60) low, Q11 and Q12 are turned on. Capacitors C52 and C53 are then switched into the circuit, changing the capacitive loading on the crystal Y1. This causes the oscillation frequency to change approximately 300 ppm.

Reset and Watchdog Timer

The System Module contains a power-on/manual reset circuit to initialize the programmed code and hardware devices on the board. The reset circuitry, U19, monitors the +5V line, and outputs a low-going pulse on U19 pin 15 as well as a high-going pulse on U19 pin 16 when the voltage on the +5V line is below +4.5V. Manual reset is also possible by pulling the reset line on J1-18C low. This is accomplished through reset switch S1 on the Power module. U19 also provides added protection to EEPROM U6 to ensure data integrity. If the +5V line falls below 4.65V, U19 inhibits any chip selects to U6 which might occur during power transients.

In addition, U19 provides a watchdog timer. The microprocessor must pulse pin 11 of U19 periodically or U19 will generate a reset. The microprocessor pulses the watchdog timer using pin U1-40.

The reset pulse is applied to microprocessor U1, to the PPI U34, and to the Backplane Board on J1-18C.

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Address Latch

The main controller on the System Module is the 80C152JB microcomputer (U1). The microcomputer obtains its instructions from the program stored in PROM U4. This can be either a 32k-byte or 64k-byte device.

The lower eight bits of the address from the micro-computer multiplex between address and data. A 74HC373 address latch (U2) is used to latch the address from the microcomputer using the microcomputer's ALE signal (U1-55). The upper eight bits of the address contain only address information, and is applied directly to all devices needing these additional address lines.

Address Decoding

A 74HC138, one-of-eight de-multiplexer (U3) is used for address decoding. The three most significant bits of the address bus (A13, A14, and A15) are used to select one of eight, 8k-byte blocks of data (non-program) memory.

The microprocessor's PSEN output signal at U1-54 is used to disable demultiplexer U3, causing all of its eight select outputs to go high so only the program PROM U4 will be selected during accesses of program memory. This prevents bus contention on the AD lines. The following devices are mapped to an 8k-byte block of data memory:

U3-15	0000-1FFFH	EEPROM (U6)
U3-14	2000-3FFFH	RAM (U5)
U3-13	4000-5FFFH	Digital Signal Processor
U3-12	6000-7FFFH	Input/Output Latches (U7, U25)
U3-11	8000-9FFFH	82C54 Counter Timer (U29)
U3-10	A000-BFFFH	82C55 Programmable Peripheral Interface (U34)
U3-09	C000-DFFFH	not used
U3-07	E000-FFFFH	not used

Program/Data Memory

Three memory components are included in the System Module: a UVEPROM (U4), a static RAM (U5), and an EEPROM (U6). The microprocessor can address two 64-kbyte memory segments; the program memory and data memory. The program memory is stored in UVEPROM U4 and is selected by a low going pulse on the microprocessor's PSEN output (U1-54).

The low going pulse on the PSEN output disables access to any data memory by disabling address decoder U3. This disables all chip selects to devices mapped to data memory locations. (Refer to the Address Decoding section for more information on devices mapped into the data memory space.)

The microprocessor executes program instructions fetched from the UVEPROM U4. The microprocessor outputs the program address on AD[0:7] and A[8:15]. The address latch latches the address on AD[0:7] when ALE goes high. The UVEPROM inputs the 16-bit address and outputs the eight-bit instruction found at the input address on the AD[0:7] lines when PSEN goes low.

Data memory is stored in static RAM U5. Data can be written to, and read from this device. However, all data is lost at power off. The RAM inputs the latched address output by the microprocessor when its chip enable input (U5-20) from address decoder U3 is low. If the RAM's OE input (U5-22) goes low, then data contained in the RAM at the input address is output to the microprocessor on the AD[0:7] lines. If the RAM's WE input (U5-27) goes low, then data on AD[0:7] is stored in the RAM at the input address.

Personality information is stored in EEPROM U6. Data can be written to and read from this device. Data stored in this device is not lost at power off. The EEPROM inputs the latched address from the micro-processor when its CE input is low. The chip enable input is generated by address decoder U3 and output on U3-15. However, the signal is routed through U19.

U19 disables an EEPROM chip enable when the board is in a reset condition. This is to ensure that no extraneous writes occur to the EEPROM during powerup or brown out conditions which would affect personality data.

If the EEPROM's OE input (U5-22) goes low while the CE is low, then data contained in the EEPROM at the input address is output to the microprocessor on the AD[0:7] lines. If the EEPROM's WE input (U5-27) goes low while the CE is low, then data on AD[0:7] is stored in the EEPROM at the input address.

Counter-Timer IC

Counter timer U29 consists of three 16-bit timer/ counters which are used for different functions de-scribed below. The microprocessor can enable, disable, and configure the counters, as well as read back counter status information from the device using its AD bus. The input clock to the device is derived by dividing by two the 14.7456 MHz clock signal out of the gate oscillator buffer U21D using D flip-flop U28. This same 7.3725 MHz clock signal is used for each counter/timer to give 135-nanosecond resolution.

Counter 0 is used for channel guard decoding. It is configured to output a 135-nanosecond pulse on U29-12 at eight times the channel guard decode frequency. This pulse is latched by D flip-flop U18A. The output of this latch is applied to the INT0 input of the micro-processor (U1-16), causing an interrupt. The micro-processor resets the latch, clearing the interrupt by pulsing U18A pin 4 using its P1.6 (U1-10) output in the interrupt service routine.

The 135-nanosecond pulse on U29-12 also causes a sample of the limited channel guard signal LIM_CG to be taken. This sample is brought into the microprocessor during the INT0 service routine on P4.7 (U1-58) and used for channel guard decoding.

The second counter/timer (counter 1) is used to generate a microprocessor interrupt. This interrupt is used by the microprocessor to generate channel guard and should occur at eight times the channel guard encode frequency. The counter is configured to send its output (U29-16) high upon timing out. This high is inverted by NPN transistor Q9, R1, and R18.

The inverted signal is then applied to the micro-processor's INT1 input (U1-18) which causes an interrupt to occur. The counter is reloaded by the interrupt service routine software. This causes U29-16 to return low, which clears the interrupt.

The third counter/timer (counter 2) is used for tone generation. When a tone is desired the microprocessor configures the counter/timer to output a square wave on U29-20 at the desired frequency. This square wave is then bandpass filtered by active filter stages U17C and U17D to remove undesired harmonics, and to create a sine wave.

A resistor divider consisting of R38 and R39 sets the level of the sine wave at U17D-14 to approximately 800 millivolts rms. The microprocessor disables the counter/timer when no tone is desired.

Programmable Peripheral Interface

Programmable **P**eripheral **I**nterface (PPI) U34 provides three additional eight-bit I/O ports. The reset generated by supervisory IC U19 is input on U34-39 and serves to reset the IC to its default state. Ports A and C are configured as output ports, and Port B as an input port.

Port C outputs are used to load the Rx and Tx Synthesizers as well as to provide serial communications with the Interface Board. Port A outputs provide an interface to the GETC in stations so equipped. The System Module loads the synthesizers and communicates with the Interface Board with the following Port C signals: RXF4/AUX2 (DATA), RXF2 (ENABLE), TXF1 (A0), TXF2 (A1), RXF1 (A2) and from Port A: SERIAL CLK (CLK). The remaining Port A and Port C outputs are used for several different interfaces.

Port B inputs several interface signals. Pullup resistors to +5V are used on all open collector type inputs. These signals are then buffered and/or level shifted where appropriate. Resistors are put in series with all of the inputs for spike protection.

Where a level shifter/buffer (U41) is not used, dual diodes are included to prevent over/under voltage conditions.

The RUS input uses an NPN transistor (Q4) to convert the signal to CMOS logic levels.

Additional I/O Latches

Additional I/O is provided by input latch U25 and output latch U7. Each of these latches are mapped to address 6000h. However, input latch U25 is enabled by a low pulse on the microprocessor's RD output while the output latch U7 is enabled by a low pulse on the microprocessor's WR output.

The input latch is used to get DC CNTRL, BATT STDBY, REM PTT, TX DISABLE, GG MON, and M3_STATUS signals onto the AD bus so they can be read by the micro-processor. The DC control currents are decoded elsewhere in the system, and the decode current is passed to the microprocessor using the DC CNTRL 1, DC CNTRL 2, and DC CNTRL 3 inputs. These are CMOS level signals, so no level shifting is required.

The BATT STDBY signal requires level shifting to convert the 22-volt high to a TTL level. This is achieved by R4 and R5. Dual diode D2 limits the signal to be within -0.7V to +5.7V to guard against over/under voltage conditions. BATT STDBY is driven high when the station is operating from AC line power and floats low due to a weak pull down resistor when the station is operating from battery power.

The 74HC377 output latch latches the data on the AD bus when the chip is selected by address decoder U3 and a low going WR pulse is received. This latched data goes to analog switch select lines used to select audio paths in the analog circuitry.

Microprocessor I/O

The microprocessor has some additional I/O pins. These pins are used to bring signals in and out of the microprocessor directly without going through any additional I/O devices such as latches or a PPI. The **LOCAL PTT** input is level shifted and buffered by U41E and brought into the microprocessor on U1-19.

The microprocessor also generates the **AUX RX MUTE** output used to mute an auxiliary receiver. The signal originates on U1-51 and is inverted by U26F. This gives an open collector active low output.

The **EXT LSD SEL**, **LINE IN SEL**, **LSACQ**, and **4W DUPLEX** signals are also generated by the microprocessor. These signals go to the analog circuitry and control audio routing through analog switches.

The microprocessor is also capable of loading electronic potentiometers U35 and U36. Each of these potentiometers contains two, 256-position variable resistors. The microprocessor must serially load all four variable resistors at the same time.

The microprocessor switches the potentiometer's select line (U1-17) high. This enables the electronic potentiometer's loading circuitry and allows the micro-processor to shift 34 bits of serial data into the electronic potentiometers, 17 bits of data into each IC.

Data is output on U1-20 and clocked into U35 and U36 on the rising edge of the clock signal generated by the microprocessor on U1-21. The microprocessor can also read back the current potentiometer settings.

When data is clocked into U35 and U36, the current potentiometer setting is clocked out and brought into the processor on U1-22. After all 34 bits have been clocked into U35 and U36, the microprocessor pulls the potentiometer's select line (U1-17) low. This ends the loading sequence, and causes the digital potentiometer's to load the new resistance value.

A/D Converter

The System Module contains an A/D converter. This is used for metering DC inputs. Four external metering inputs are accommodated. These include **PWR SNSR**, **TX MTR+** relative to **TX MTR-**, **RX MTR+** relative to **RX MTR-**, and **EXT JCK**.

The **PWR SNSR** input will accommodate a DC level between zero and +5V relative to analog ground. The input is protected from over voltage conditions by dual diode D7.

The Control Shelf routes **TX MTR+** and **TX MTR-** into a differential amplifier consisting of U17A, R140, R142, R145, and R146. This amplifier removes any common-mode voltage. The output of this differential amplifier is actually measured and must be between zero and +2.9 Volts.

The **RX MTR+** input is assumed to be between zero and +5V relative to analog ground. No conditioning is performed except for dual diode D3 that protects from over/under voltage conditions.

The **EXT JCK** input is designed to input signals between zero and +10V relative to **AGND**. Operational amp U17B provides a high input impedance and buffers the input signal. The output of this amp goes through a voltage divider network composed of R3 and R6 that divides the DC level by two. This signal is then routed to the multiplexer U33.

Analog multiplexer U33 gates one of four inputs to the A/D converter U27. The microprocessor determines which input is selected using U1-52 and U1-57. The microprocessor starts an A/D conversion by putting a rising edge on U27-5. U27 then converts the DC input voltage selected on U33 to a digital value.

The converted digital value is clocked out of U27 sequentially by the microprocessor, beginning with the most significant bit. The microprocessor selects U27 by setting U27-5 low. When the A/D converter is selected it puts the MSB of the eight bit conversion data on U27-6. This is read by the microprocessor. Successive data bits are clocked out of the A/D converter on falling edges of its CLK input (U27-7).

When all eight bits have been clocked out, the A/D converter is deselected, and the next conversion cycle begins by the microprocessor setting U27-5 high.

DSP Interface

System Module 19D902590G3 is equipped with plugs to accommodate Digital Signal Processor (DSP) "piggyback" board 19D902667G1. The board plugs into J2 and J3 of the System Module.

The microprocessor communicates with the DSP board through its eight-bit AD[0:7] bus, using a dual port RAM located on the DSP board. This memory is mapped into an 8k-byte data memory segment using address decoder U3. Data can be written to and read from any of the 256 byte locations that can be addressed by AD[0:7].

The DSP board contains an address latch to latch the address information on AD[0:7] when ALE goes high. When the DSP CS is low and the microprocessor WR output is low, the data on AD[0:7] is written into the latched DSP data memory segment address. When DSP CS is low and the microprocessor RD output is low, data on AD[0:7] is read into the microprocessor U1 from the latched DSP data memory segment address.

Two handshake lines used for the DSP interface for synchronization are **DSP TBLF** and **DSP RBLE**. When the DSP has written a message to the dual port RAM, it signals microprocessor U1 by asserting DSP TBLF low. The microprocessor then reads the message from the dual port RAM and then resets DSP TBLF high to tell the DSP that it is ready for another message.

When the microprocessor wants to send a message to the DSP it first looks at the **DSP RBLE** input. A high on this input indicates that the DSP receive buffer is empty and it is ready to accept a new message. When the microprocessor has written the message to the dual port RAM, it asserts **DSP RBLE** low to signal the DSP that it should read the new message. The DSP resets DSP RBLE high after it has read the message.

The microprocessor can reset the DSP board by setting U1-7 high. The high is inverted by Q10, and the resulting low resets the DSP board.

RS232 Interface

The System Module has an RS232 serial port for programming and diagnostics. RS232 data is received on the **PGM RXD** input and converted to TTL levels by U22A. The TTL data is brought into the micro-processor's internal UART on pin U1-14. Transmit data is output on U1-15 by the microprocessor, and level shifted to RS232 levels by U22B. The RS232 data is output on **PGM TXD**.

GSC Interface

A high speed serial interface that is referred to as a global serial channel (GSC) is also included on the System Module. Data is transferred bidirectionally over an RS485 differential pair made up of COMM+ and COMM.

When the microprocessor wants to send data over the GSC, it enables the drivers in U24 by outputting a low on U1-6. Data is generated internally in the micro-processor and output on U1-5. The data is converted to RS485 levels and output on the GSC by U24.

The receiver section of U24 is always enabled so that the microprocessor's receiver can monitor the transmitted data. This monitoring is to check for collisions on the GSC created by multiple GSC nodes transmitting simultaneously.

U24 converts received data to TTL levels and outputs them on U24-1. The microprocessor brings the TTL level data into its receiver on U1-4 for message decoding.

Transmitter Interface

The System Module is responsible for loading the Tx Synthesizer Module with its' proper frequency information. When the micro-controller sees a PTT from an enabled source, it first drives ANT RLY active. This switches the antenna switch in stations with this option and also applies power to the Tx synthesizer oscillator circuit. Next, data is shifted into the Tx Synthesizer using A2, A1, A0, CLK, and DATA. After the TX Synthesizer has been loaded with data, ENABLE goes active for 10 mS to allow the TX Synthesizer PLL circuit time to acquire frequency lock. At the end of this ENABLE period, the micro-controller samples the TX Synthesizer status bit supplied by the Interface Board. If there is no fault (synthesizer locked) then the micro drives TX OSC CNTRL (PA KEY) active which turns on the RF PA. Upon reset or a channel change, the System Module must also set the PA power pot by sending appropriate data to the Interface Module.

Audio for transmission is output on the **TX AUDIO HI** and **TX AUDIO LO** outputs. Channel guard is summed into **TX AUDIO HI.**

Receiver Interface

At power up or upon channel change, the RX Synthesizer is programmed in the same manner as the TX Synthesizer. Carrier activity on the selected channel is sensed by the receiver's squelch circuitry and applied to the System Module on the **CAS** input. This active high input is level converted by Q8, and applied to the microprocessor on U1-23. The microprocessor then routes audio according to the station's configuration programming.

Local Controls

The System Module has three switches and LEDs for local control. Switch S2 is a REMOTE PTT switch. When not activated, R23 pulls the line to +5V. When activated, S2 pulls the line to ground. This switch is input on pin 7 of input latch U25. The line is also routed to the external connector to allow an external module to activate the remote PTT input. A low on this input causes the microprocessor to react as though a PTT has been received over the line.

Switch S3 is a TX DISABLE switch. When not activated, R136 pulls the line to +5V. When activated, the switch pulls the line to ground. This switch is input on pin 8 of input latch U25. When S3 is activated, the microprocessor inhibits all transmissions.

Switch S4 is a CG MONITOR switch. When not activated, R137 pulls the line to +5V. When activated, the switch pulls the line to ground. This switch is input on pin 9 of input latch U25. The line is also routed to the external connector. This allows an external module to activate the CG MONITOR input, or to examine the state of the CG MONITOR input. A low on this input causes the microprocessor to switch into channel guard monitor.

The System Module concurrently activates the ANT Relay output and LED DS1. When the System Module is in CG MONITOR, it lights LED DS3 by outputting a high on U1-66. This high is inverted by U2D. This allows current to flow through DS3, turning on the LED.

Putting the System Module in the transmit disable mode lights LED DS2 by outputting a high on U1-67. This high is inverted by U26C. This allows current to flow through DS2 to turn on the LED.

CG Filter, High Pass and De-emphasis Amps

Receiver audio is applied to the System Module "VOL/SQ HI" port on J1-2B. U37A buffers the input signal and removes any Dc bias. With an input of 1 Vrms at 1000 Hz, the output is typically 2 Vrms and is supplied to three places; channel guard reject filter, the DSP board through DSP unfiltered audio, and channel guard decode.

U30A is a unity gain notch-filter, centered at 205 Hz. The filter provides 25 dB of attenuation. U30B, U30C, and U30D form a sixth order, unity gain high-pass filter, with a cut-off frequency of 280 Hz. U37B is a +1/-3 dB de-emphasis filter that rolls the audio off at 6 dB-per-octave in the frequency range from 300-3000 Hz.

With 1 Vrms into VOL/SQ HI, the output of U37B will be 750 millivolts rms. This output is supplied to four places; U8A, TX Audio out, Line Audio out, and the summing amplifier with the optional auxiliary receiver input. U8A is controlled by the microprocessor to switch between MIC and VOL/SQ audio to the DSP. The combination of U37A, U30A, U30B, U30C, U30D, and U37B provide the frequency envelope-shaping requirements (roll-off) as shown in Figure 1.

The TX Audio Out circuit consists of U15, U36A, U8C, and U37D. U15 is an analog multiplexer which is controlled by the microprocessor. Any of the following signals can be connected to the TX AUDIO HI output; LOCAL MIC, VOL/SQ, DSP LINE/TX AUDIO, DSP TX AUDIO, External High Speed Data, LINE Input, open (battery alarm), and Ground (for no transmission). U8C is an analog mux which is controlled by the microprocessor to sum CG into the TX AUDIO output and increase the TX AUDIO gain on U37D.

Battery Alarm/Morse Code is summed with the output of U15. This allows for transmission of the alarm signal when other signals are present. U36 is a dual-digital potentiometer which is controlled by the microprocessor, and adjusts the transmit audio level. U37D is a gain stage which drives the TX AUDIO HI output. The level at TX AUDIO HI (J1-5C) and TX AUDIO LO (J1-6C) is adjustable between 40 and 250 millivolts rms.

U37C is the +2/-8 dB de-emphasis filter which provides a 6 dB per octave roll off from 300-3000 Hz for the local intercom or speaker audio. With a rated input of 1 Vrms at 1000 Hz, the output level of this filter is 750 millivolts rms. This filter, in combination with U37A, U30A, U30B, U30C, and U30D provide the frequency response shown in Figure 2.

U32 is the analog multiplexer for the INTERCOM Audio output. It allows for selection of VOL/SQ audio, LINE Input audio, Voice Guard summing, and DSP LINE/TX AUDIO. Amplifier U31C sums the multiplexed audio with Voice Guard tone. The resulting signal is applied to J1-7A.

CG/LSD Decode Filter

Received audio is coupled through a low pass filter to remove the audio, leaving only Channel Guard (CG) or Low Speed Data (LSD) information. A hard limiter then converts the signal into a digital square wave. The square wave is decoded in software as well as the 135-degree phase shift for STE.

U9A is a gain stage which supplies two frequency-dependent, negative resistor (FDNR) circuits. The first FDNR consists of U10A and U10B, and has a cut-off at 205 Hz. The second FDNR, formed by U10C and U10D, has a cut-off at 230 Hz.

U11B is a low pass filter which provides added attenuation in the 300-3000 Hz range. These elements combine to provide 35 dB of attenuation for frequencies above 310 Hz. The resulting frequency response is shown in Figure 3.

U11A, D5, and Q2 combine to convert the analog signal at the U11B output to a 0-5 Vdc square wave. This square wave is then supplied to U18B to be read and decoded by the microprocessor.

CG/LSD Encode Filter

U12C is used to select between external low speed data or WALSH bits. The WALSH bits are created by the microprocessor on pins U1-64 and U1-65, and form a rough sine wave. This signal is coupled through U9C to provide some gain.

U16A, U16B, U16C, and U16D form two FDNR circuits which have the same response as described in the CG/LSD DECODE FILTER section. U9D provides gain and drives U35A. U35A is a digital potentiometer which provides level adjustment and is controlled by the microprocessor. Also, U9B has a 3.3 k-ohm source impedance to allow a separate source to drive Channel Guard HI. This filter has the same response as shown in Figure 3.

Local Mic Input

The local microphone input at J1-3A and J1-3B supplies 12-Volts dc level to power the microphone. This input is buffered through U13A, which removes the DC bias and amplifies a 100-millivolts rms input for a 775-millivolts rms output.

Battery Alarm/Morse Code

The Battery Alarm/Morse Code tones are generated using U29, U17C, and U17D. U29 is a Clock Timer which creates a square wave at the required frequency. C113 and R39 form a high pass filter to provide DC blocking. U17C is second order low pass filter and U17D provides gain. These components combine to provide the response shown in Figure 4.

The output of U17D sources the signal to U31B and U15. U15 is the TX AUDIO multiplexer discussed earlier in this section. U31B is an amplifier to sum the Battery Alarm signal with the Voice Guard Alert tone, which is then transmitted to the LINE Output.

Line Audio And Compression

The LINE output circuit consists of U14, U8B, U36B, U31D, U13B, and U31A. The analog multiplexer U14 is used to connect one of the following signals to the LINE driver U31D; LOCAL MIC, VOL/SQ, auxiliary receiver, aux receiver/VOL/SQ, DSP LINE/TX audio, MODEM LINE Data, open and Ground. The open state is to transmit Battery Alarm or Voice Guard Alarm.

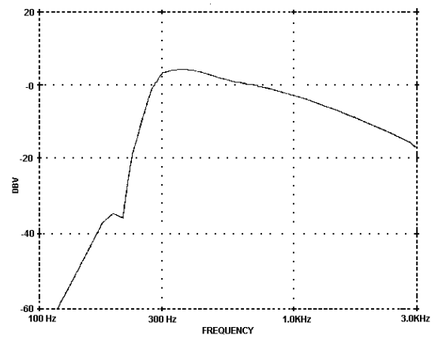


Figure 1 - Channel Guard Tone Reject (+1, -3 dBV)

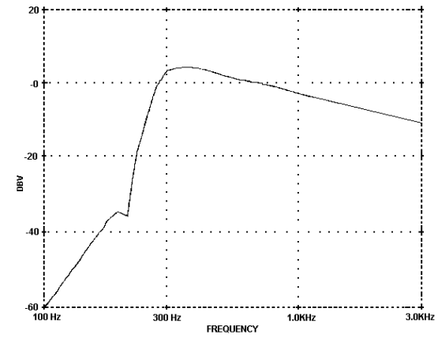


Figure 2 - Channel Guard Tone Rejct Filter (+2, -8 dBV)

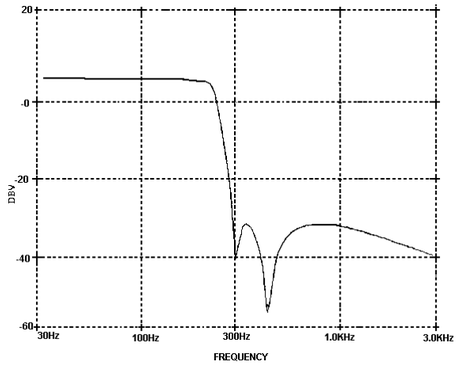


Figure 3 - Channel Guard Encode/Decode Filter

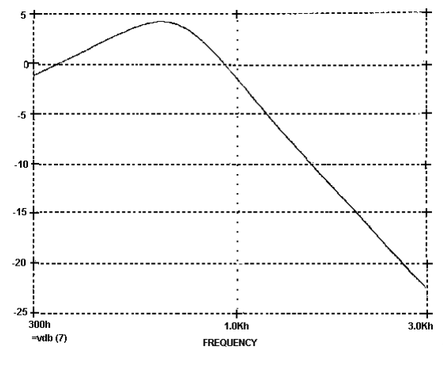


Figure 4 - Battery Alarm/Morse Code Band-Pass Filter

U31A sums the aux receiver audio with the VOL/SQ audio. U36B is a digital potentiometer and controls the audio level into the line driver U31D. The level at LINE A (J1-4B) and LINE B (J1-4A) is adjustable between -20 dBm and +11 dBm.

The LINE IN audio is selected from LINE A and LINE B in a two-wire system, and from DUPLEX LINE A and DUPLEX LINE B in a four-wire system. Each input has a 600-ohm impedance to match the line impedance. U12B selects between two-and four-wire audio.

Digital potentiometer U35B sets the level applied to the line compensation filter U13B. This filter can be set up to compensate for high frequency roll-off on long lines by removing R16. This modification should be used when roll-off in the 2500 to 3000 Hz range is more than 10 dB below the 400 to 600 Hz level.

Following U13B is the compression circuit consisting of U13C, U13D, D6, and Q3. LINE IN audio from U13B is applied to a network composed of R65, Q3, R75, and R76. After being amplified by U13C, the output is supplied to four places: Line Output, TX Audio output, Intercom audio, and D6.

This compensation circuit is only effective in stations using Group 1 System Modules (no DSP) or Group 2 modules programmed for DC Remote Control. For all other applications, audio routing bypasses the compensation filter.

The output of amplifier U13C is rectified by D6 which charges C25. U13D amplifies the voltage on C25 and provides a DC offset to the gate of Q3. Q3 serves as a variable resistor in the voltage divider composed of R65 and Q3 which limits the input to U13C. R75 and R76 serve to reduce distortion across the voltage divider.

This circuit normally operates in a linear fashion with Q3 turned off which appears as a high resistance. When higher than normal audio is received at U13B, the amplification of U13C is rectified by D6, increasing the voltage across C25.

The increased voltage across C25 through U13D starts turning on Q3 reducing its drain to source resistance, which in turn, lowers the audio to U13C. Since this affects not only the output of U13C, but the turn-on voltage of Q3 from U13D, a steady audio output is provided.

NOTE

Service Note: The compressor can be disabled by removing Q3. The compressor is typically disabled when shipped from the factory. It is preferable to use the compressor function on the DSP board. If this hardware compressor is used, install Q3 (19A703795P1; sim to 4416) on System Board (19D903771G1).

DSP BOARD

The **D**igital **S**ignal **P**rocessing (DSP) Board utilizes both digital and analog integrated circuits (IC's) to offer a compact, flexible, and reliable solution for audio signal analysis and modification. Most of the components are surface mounted.

The DSP Board operates with two channels of audio. It conditions the audio inputs, digitizes the audio, and processes the audio data in software. The DSP Board then sends the transformed audio to analog outputs, and the signal analysis information to its digital output.

Audio inputs from the System Module board are **DSP_FILT_VOL/SQ**, **DSP_UNFILT_VOL/SQ**, and **DSP_LINE_IN**. These signals are selected and conditioned through U10, U11, and U15. The signals are then sampled and digitized by U4 and U5. The digital audio data is then applied to U1 for processing. After processing, the audio data is returned to U4 and U5 for digital to analog conversion. The transformed audio is applied to the System Module board on **DSP_TX_AUD** and **DSP_LINE/TX_AUD**.

All pertinent information from the DSP analysis of the audio is communicated digitally to the System Module through the dual port RAM, U12. Messages are written to this piece of memory by the DSP micro-computer, U1. The messages are read from the memory by the System Module (via the digital signals of connector P3).

For clarity, the DSP circuitry is analyzed in the following order:

1) DSP and supporting circuitry
2) Analog Input/Output
3) Parallel communication port

DSP Microprocessor

The DSP Board performs its functions in the ADSP-2101 Digital Signal Processing Microcomputer, U1. This chip requires external hardware to function.

Crystal (Y1) provides the 8.192 MHz clock required by the DSP microprocessor. Capacitors C16 and C17 provide the loading required for reliable start-up and stable oscillation.

The DSP microprocessor can read or write to both internal and external data memory. Two identical 8K X 8 static RAM's (U2 & U3), are used to form an 8K X 16 external data memory space. External 16-bit data memory is applied to the DSP on D8-D23. U3 holds the most significant byte (MSB), and U2 holds the least significant byte (LSB).

For a single external memory address, U3 stores D23 through D16, and U2 stores D15 through D8. A 16-bit word is formed in order to maintain compatibility with the processor's internal 1K X 16 data memory architecture.

When the processor attempts to address data memory which exceeds that which is available internally (1K X 16), the address bus, A12 through A0, sets up an external address. The data memory is enabled by a low on **/DMS**. A read or write is activated by a low on the **/RD** or **/WR** pin. The external data memory access is completed when address pins return to their high impedance state, **/RD** or **/WR** returns to high, and **/DMS** rises to logic high.

DSP microprocessor U1 operates from a 2K internal program memory. This program RAM is volatile; it is lost during power-off sequences. Therefore, it is necessary to have non-volatile memory to safely hold the DSP Board code. The 16K X 8 EPROM (U6) performs this function.

Upon reset, or during a "re-boot", up to 2K x 24 of internal program memory is loaded from this external "BOOT EPROM." The Boot EPROM, U6, holds up to eight different pages which can be loaded. The selection of a 2K-page of code is software-controlled except during reset when boot page zero is always loaded.

In essence, boot memory page loading is a sequence of "read" cycles. The BMS pin goes low in order to enable the boot memory chip. Addresses are sequenced on lines A0 through A13, D22 and D23. The **/RD** pin activates the data bus, D15 through D8, for each transfer of program memory into the internal program memory space.

The boot EPROM circuitry also includes resistors R1 and R2. These resistors are zero ohms, and are equivalent to jumper wires. If the capability of 8 boot pages is necessary, R2 is removed, and R1 is installed on the board. In this case, U6-pin 1 acts as an extra address pin which is connected to D23. If the capability of 4 boot pages is necessary, R1 is removed, and R2 is installed on the board. In this case, U6 pin 1 acts as a program pin, and is tied off to five volts.

Analog Inputs

The DSP Board inputs and processes audio from both the receiver and the line simultaneously. There are two possible receiver audio input settings and two possible line audio input settings. These are:

(1) **DSP_FILT_VOL/SQ** or **DSP_UNFILT_VOL/ SQ** input, and

(2) Two-wire line input or four-wire line input.

This audio selection is actuated directly by the DSP but is user-programmable. The DSP uses the address multiplexer, U8, to select U7, a D-flip flop register. This is accomplished by setting A13-A11 to binary 100 when **/PMS** goes low. Such a sequence will cause U8-pin 14 to go low, enabling data to pass through the D-flip flops upon **/WR** going low and then high. D8 and D9 are written to the outputs of U7 (pins 2 and 5) as **VOL/SQ_SEL** and **CANCEL_SEL**.

Depending upon these signals, digitally-controlled analog switches (U10) route the appropriate signals to achieve the final audio input settings described above. If **VOL/SQ_SEL** is a logic high, **DSP_UNFILT_VOL/ SQ** is selected; otherwise **DSP_FILT_VOL/SQ** is selected. If **CANCEL_SEL** is a logic high, four-wire operation is selected. If not a logic high, two-wire operation is selected.

Each audio channel selection requires proper voltage level adjustment to insure an optimal conversion to the digital domain where it will be processed. This conversion is performed by codecs U4 and U5. In other words, the analog audio signals are conditioned to assure that their dynamic ranges can be accommodated by the codecs. The codecs will neither be under-driven nor saturated. This results in a digital audio signal with uniform Signal-to-Noise Ratio (SNR) following the codec A/D conversion.

Filtered Receiver Input Conditioning

Filtered receiver input comes from the System Module following de-emphasis and channel guard reject filtering at a maximum of 1.16 Volts rms. This input channel requires no amplification to assure that codec U4 utilizes its dynamic range efficiently.

The amplification factor is determined by resistors R5 and R6. The gain is one. Therefore, the maximum input voltage to the codec is 1.16 Volts rms.

Four-Wire Line Input Conditioning

Four-wire line input comes from the **DPLX** line input pair of the Control Shelf when it is in a four-wire configuration. Its audio is not in contention with audio which is leaving the station because there are two lines independently dedicated for the output signal.

The line audio level-adjustment is able to attenuate a 2.47 Volts rms (+11 dBm) signal, and amplify a 77.3 mVrms (-20 dBm) signal to the maximum input level of a codec (approximately 1.4 Volts rms). This is to compensate for up to 30 dB of line loss that can occur between the Remote Control Unit and the station.

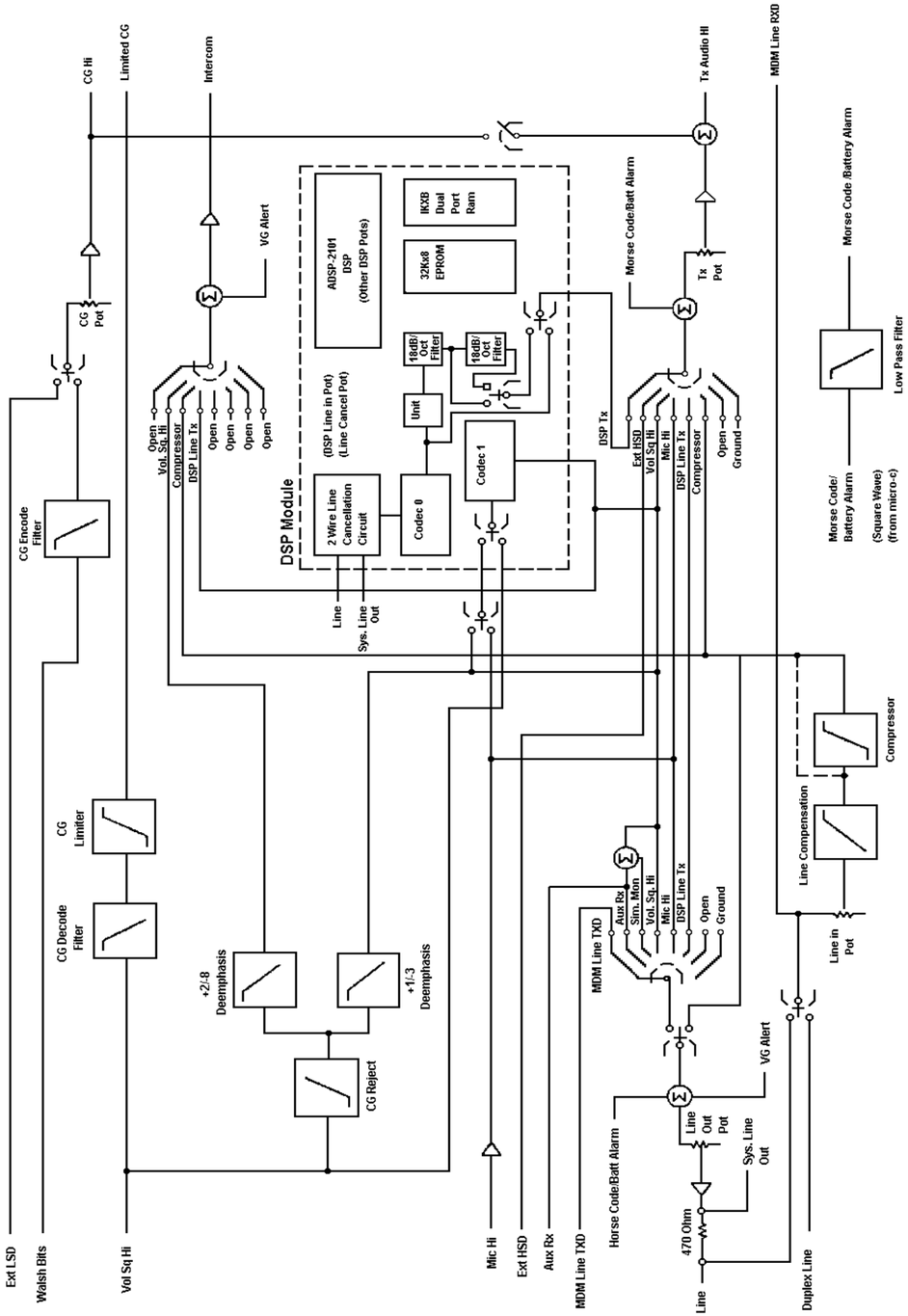


Figure 5 - Control Module Analog Section

In the four-wire configuration, **DSP_LINE_IN** is pro-pagated to TP1 with only a gain of 1.09 provided by the differential instrumentation amplifier circuit of U11(A,B,C) and R12-R17. This occurs because the amount subtracted from **DSP_LINE_IN** is **AGND** (U10A pin 13).

Between TP1 and TP2 there is a digitally controlled variable gain stage. The gain stage is composed of U11D, U15(1), R18, and R20. The DSP addresses (and serially loads) a resistance from 0 to 10K-ohms into the dual programmable potentiometer, U15. The digitally-controlled impedance, along with R18 and R20, form a gain through operational amplifier U11D.

The DSP uses address multiplexer U8 to select U7, a D-flip flop register. This is accomplished by setting A13-A11 to binary 100 when **/PMS** goes low. Such a sequence will cause U8-pin 14 to go low, enabling data to pass through the D-flip flops upon **/WR** going low and then high.

Data is written to the D10, D11, and D15 outputs of U7 (pins 6, 9, and 19) known as **POT_CLK, POT_LOAD_EN**, and **POT_IN** which directly control U15. **POT_CLK** is a serial clock. **POT_IN** is serial data. **POT_LOAD_EN** is a serial load enable. During a "load" cycle, **POT_LOAD_EN** is held high. Seventeen **POT_IN** values are set up and held with respect to the rising edges of **POT_CLK**. The first value loaded into the dual programmable potentiometer is a "don't care" value. The following sixteen values comprise two 8-bit wiper positions. Wiper 1 gets loaded before wiper 0. Loading is specified from MSB to LSB.

Two-Wire Line Input Conditioning

Two-wire line input comes from the Line input of the System Module when it is in a two-wire configuration. This audio is in contention with audio which is leaving the station on the same two-wire pair. The DSP Board must cancel out the interfering output audio from the input. In addition, it must amplify the input signal to account for the line loss of up to 30 dB that can occur between the Remote Control Unit and the station.

Cancellation of transmit audio from receive audio on the two wire pair is accomplished by the differential instrumentation amplifier consisting of U11(A,B,C), R11-R17, and the DSP-controlled resistance through U15(0) and R10. The **SYSBD_LINE_OUT** (a DSP Board input signal) is limited by U18A and level adjusted through the programmable potentiometer, U15(0), (as explained above) and then subtracted from the line input signal.

After subtraction, the remaining input (received audio) is level adjusted by the remaining programmable potentiometer U15(1) exactly as in the four-wire case.

DSP Analog Outputs

The Rx output of codec U5, TX CODEC RX, passes through U16-B for pre-emphasis and hard limiting. Limiting action occurs when the instantaneous AC voltage exceeds the DC bias set by R34, R36, and R37, at which point D1 becomes forward biased placing it in the feedback loop of U16-B. Due to the V-I characteristic of the diode, limiting action occurs. U16-B also provides +6 dB/octave pre-emphasis for transmitted audio in the 300 Hz to 3 kHz band. The pre-emphasis meets the EIA standard of +1/-3 gain flatness in its passband.

Following the pre-emphasis and limiter, U16-C forms a third order low pass filter stage required by FCC regulations to filter the harmonics created by the preceding limiter. R35 and C29 compose a passive first order low pass while active filter U16-C provides an additional two poles for this filter stage. Following U16-C is another filter stage consisting of a second order passive low pass and a second order active low pass built around U16-D.

Analog switch U17 selects which filter stage output, if any, is routed to the transmitter. Depending upon the transmit frequency band, the FCC requires different filter characteristics for the post-limiter filter. The output of analog switch U17-B DSP TXAUD is routed to P2-7 where it connects to the System Module.

The RX output of U4 pin 2 DSPLINE/TXAUD is routed to P2-8 where it connect to the System Module. This audio output typically drives the line out circuits on the System Module.

Parallel Communications Hardware

The DSP Board is equipped with a full duplex, parallel interface for communications between the System Module microprocessor and the DSP microprocessor chip. Communications are accomplished through a dual port RAM, U12.

Byte-wide messages are passed between System Module and DSP chip by reading and writing data upon this common piece of memory.

The external eight-bit System microprocessor can read and write to the dual port RAM. A 74HC373 address latch (U13) is used by the 8-bit host to latch the address (AD7-AD0). The host uses its ALE signal to perform the actual clocking into the latch.

Once ALE has returned to logic one, AD7-AD0 become bi-directional data pins. During a "write" cycle, the host sets up data on AD7-AD0. During a "read" cycle, the System Module microprocessor releases the data lines AD7-AD0 into their high impedance state.

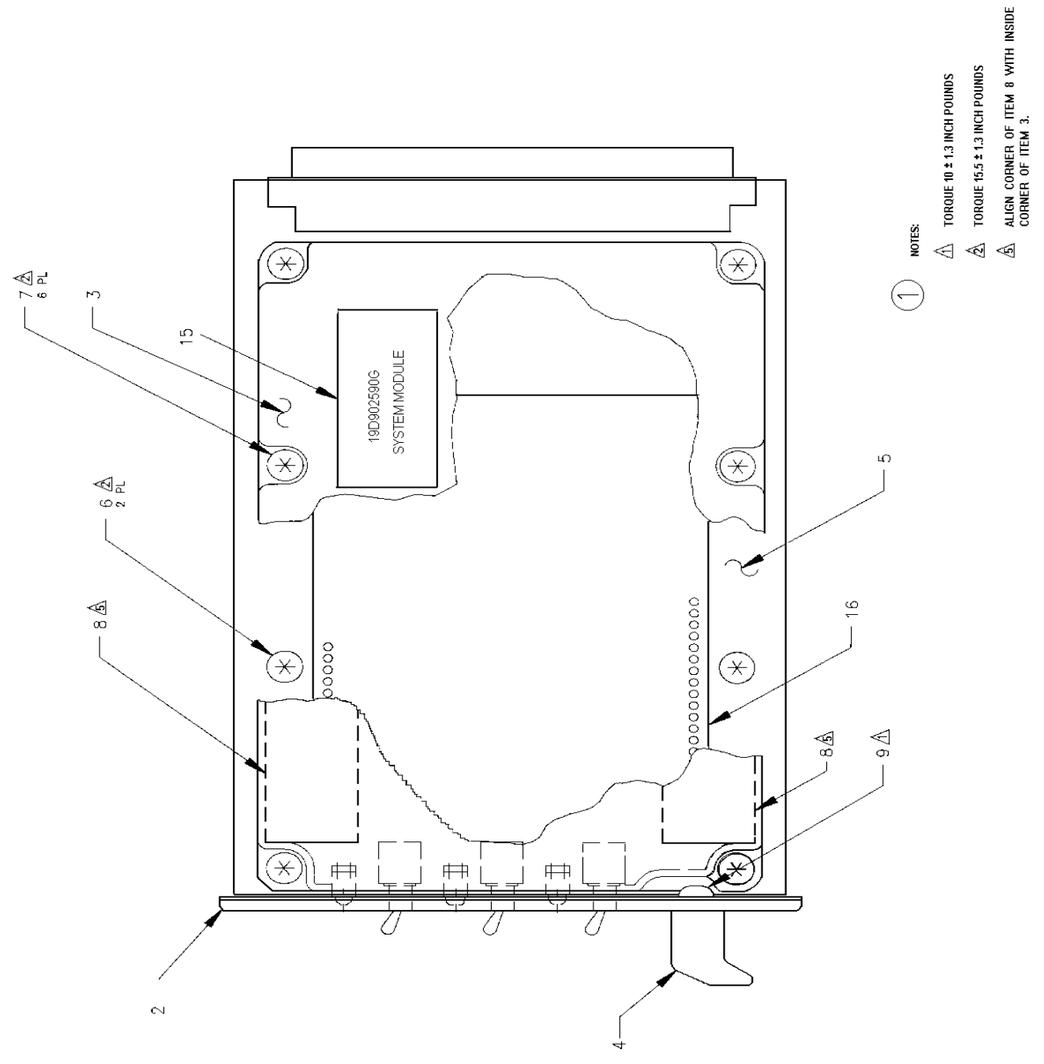
Finally, the System Module's low-going **/UPRD** or **/UPWR** pulse executes the desired read/write function. Note that reading and writing is only accomplished when the **DSP_CS** signal is held low. In this way, the System Module microprocessor exclusively selects the dual port memory space to prevent contention upon the multiplexed address and data bus.

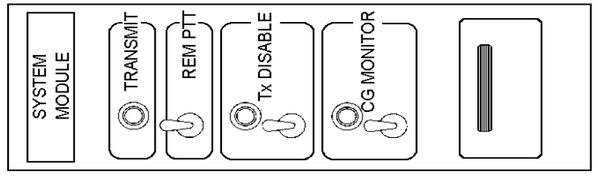
The DSP chip reads and writes from the dual port RAM by first selecting its communication memory space. This is accomplished by setting A13-A11 to binary 010 when PMS goes low. Such a sequence will cause U8 pin 13 to go low and thus enable the dual port RAM, U12. Once enabled, the communications memory is accessed with address lines A9-A0 and data lines D15-D8, in conjunction with a low-going **/RD** or **/WR** pulse.

The DSP chip (U1) and host processor coordinate message handling through the **RBLE** and **TBLF** flags. The DSP chip sets **TBLF** by writing to location 3FFH of the dual port RAM; it clears **RBLE** by reading from location 3FEH of the dual port RAM.

Similarly, the host microprocessor can clear **TBLF** by reading from location 3FFH of the dual port RAM. It then sets **RBLE** by writing to location 3FEH of the dual port RAM. (Note that a flag is set when it is low; it is clear when it is high.) This way, both microprocessors can monitor flag conditions in order to keep from trying to access the same locations in memory at the same time.

Tri-state buffer U9 is used by the DSP microprocessor in order to read the **RBLE** and **TBLF** flags. This alleviates the possibility of contention on the DSP's data bus D15-D8. The **RBLE** and **TBLF** flags are read by first selecting U9. This is accomplished by setting A13-A11 to binary 100 when **/PMS** goes low. Such a sequence will cause U8-pin 14 to go low and thus enable data to pass through the tri-state buffer upon **/RD** going low. U9, pins 2 and 3 appear on D8 and D9, and are latched into U1 when **/RD** returns high.





SYSTEM MODULE
19D902590G1-G3

(19D902590, Sh. 1, Rev. 3)

SYSTEM MODULE

19D902590G1 - M IIe System Module
19D902590G2 - M IIe System Module with DSP
19D902590G3 - M III System Module with DSP

SYMBOL	PART NO.	DESCRIPTION
2	19D902485P1	Chassis.
3	19D902486P1	Cover.
4	19D902555P1	Handle.
6	19A702381P506	Screw, thread forming: TORX, No. M3.5 - 0.6 x 6.
7	19A702381P513	Screw, thread forming: TORX, No. M3.5 - 0.6 X 13.
8	19B232682P20	Pad. (Used in G2 and G3).
9	19A702381P508	Screw, thread forming: No. 3.5-0.6 x 8.
15	19B235310P1	Nameplate.
16	19D902667G1	Digital Signal Processor, (Used in G2 and G3).
18	19D903771G1	System Board (See below).
		SYSTEM BOARD 19D903771G1
		- - - - - - - - - - CAPACITORS - - - - - - - - -
C1	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C2	19A702052P14	Ceramic: 0.01 µF ± 10%, 50 VDCW.
C3	19A702061P13	Ceramic: 10 pF ± 5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C4	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C5	19A702052P26	Ceramic: 0.1 µF ± 10%, 50 VDCW.
C6 and C7	19A702052P114	Ceramic: 0.01 µF ± 5%, 50 VDCW.
C8	19A705205P5	Tantalum: 6.8 µF, 10 VDCW; sim to Sprague 293D.
C9	19A702052P28	Ceramic: 0.022 µF ±10%, 50 VDCW.
C10 and C11	19A702052P114	Ceramic: 0.01 µF ± 5%, 50 VDCW.
C12	19A702052P14	Ceramic: 0.01 µF ± 10%, 50 VDCW.
C13	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C14	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C15	19A702052P124	Ceramic: 0.068 µF ± 5%, 50 VDCW.
C16	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C17	19A705205P2	Tantalum: 1 µF, 16 VDCW; sim to Sprague 293D.
C18	19A702052P24	Ceramic: 0.068 µF ± 10%, 50 VDCW.
C19	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C21	19A702061P77	Ceramic: 470 pF ± 5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C22	19A702052P14	Ceramic: 0.01 µF ± 10%, 50 VDCW.
C23	19A702052P26	Ceramic: 0.1 µF ± 10%, 50 VDCW.
C25	19A705205P111	47 µF ±10%, 10VDCW; sim to Sprague
C27 and C28	19A705205P111	47 µF ±10%, 10VDCW; sim to Sprague
C29 thru C36	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C38	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C39	19A705205P5	Tantalum: 6.8 µF, 10 VDCW; sim to Sprague 293D.
C40	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C42 thru C45	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C46	344A3431P1	Monolithic: 1.0 µF +80/-20%, 16 VDCW.
C47 thru C50	19A702052P114	Ceramic: 0.01 µF ±5%, 50 VDCW.
C51	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C52	19A702061P37	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C53	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C58	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C59 and C60	19A702052P122	Ceramic: 0.047 µF ±5%, 50 VDCW.
C61	19A702052P26	Ceramic: 0.1 µF ± 10%, 50 VDCW.
C62 thru C67	19A149791P1	Metallized Polyproylene: 0.022 ±1%, 100 VDCW.
C68 thru C71	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C72 and C73	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C74 thru C78	19A702052P14	Ceramic: 0.01 µF ±5%, 50 VDCW.
C79	19A702052P114	Ceramic: 0.01 µF ±5%, 50 VDCW.
C80 thru C84	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C87 thru C95	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C96 thru C98	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C99	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C100 and C101	19A702052P14	Ceramic: 0.01 µF ± 10%, 50 VDCW.
C102	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C103	19A702052P114	Ceramic: 0.01 µF ±5%, 50 VDCW.
C104	19A705205P111	47 µF ± 10%, 10 VDCW; sim to Sprague
C105 thru C108	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C109 and C110	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C111	19A702052P114	Ceramic: 0.01 µF ±5%, 50 VDCW.
C112	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C113	19A702052P114	Ceramic: 0.01 µF ± 5%, 50 VDCW.
		- - - - - - - - - - DIODES - - - - - - - - - -
D1 thru D8	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
		- - - - - - - - INDICATING DEVICES - - - - - - -
DS1 thru DS3	19A703595P10	Diode, Optoelectric: Red; sim to HP HLMP-1301-010.
		- - - - - - - - - - JACKS - - - - - - - - - -
J1	19B801587P7	Connector, DIN: 96 male contacts, right angle mounting; sim to AMP 650887-1.
J2 and J3	19A704852P334	Connector, printed wire board.
		- - - - - - - - - - INDUCTORS - - - - - - - - - -
L1 and L2	19A705470P53	Coil, fixed.
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q2	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q4 and Q5	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q6	344A3855P1	Silicon: NPN: sim to PZT2222A.
Q7	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q8	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q9 and Q10	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q11 and Q12	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R2	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R3	19A702931P301	Metal film: 10K ohms ±1%, 200 VDCW, 1/8 w.
R4	19B800607P153	Metal film: 15K ohms ±5%, 1/8 w.
R5	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R6	19A702931P301	Metal film: 10K ohms ±1%, 200 VDCW, 1/8 w.
R7	19A702931P249	Metal film: 3160 ohms ±1%, 200 VDCW, 1/8 w.
R8	19A702931P313	Metal film: 13.3K ohms ±1%, 200 VDCW, 1/8 w.
R9	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R10	19B800607P391	Metal film: 390 ohms ±5%, 1/8 w.
R11	19B800607P562	Metal film: 5.6K ohms ±5%, 1/8 w.
R12	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R13	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R14	19B800607P272	Metal film: 2.7K ohms ±5%, 1/8 w.
R15	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R16	19B800607P1	Metal film: Jumper.
R17	19A702931P369	Metal film: 51.1K ohms ±1%, 200 VDCW, 1/8 w.
R18	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R19	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R20	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R21	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R22	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R23	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R24	19B800607P122	Metal film: 1.2K ohms ±5%, 1/8 w.
R25	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R26	19A702931P384	Metal film: 73.2K ohms ±1%, 200 VDCW, 1/8 w.
R27	19A702931P388	Metal film: 80.6K ohms ±1%, 200 VDCW, 1/8 w.
R28	19A702931P358	Metal film: 39.2K ohms ±1%, 200 VDCW, 1/8 w.
R29	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R30	19A702931P384	Metal film: 73.2K ohms ±1%, 200 VDCW, 1/8 w.
R31	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R32	19A702931P369	Metal film: 51.1K ohms ±1%, 200 VDCW, 1/8 w.
R33	19A702931P325	Metal film: 17.8K ohms ±1%, 200 VDCW, 1/8 w.
R34	19A702931P350	Metal film: 32.4K ohms ±1%, 200 VDCW, 1/8 w.
R35	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R36	19A702931P382	Metal film: 69.8K ohms ±1%, 200 VDCW, 1/8 w.
R37	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R39	19A702931P401	Metal film: 100K ohms ±1%, 200 VDCW, 1/8 w.
R40	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R41	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R42	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R43	19B800607P684	Metal film: 680K ohms ±5%, 1/8 w.
R44	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R45	19B800607P683	Metal film: 68K ohms ±5%, 1/8 w.
R46	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R47 and R48	19B800607P681	Metal film: 680 ohms ±5%, 1/8 w.
R49	19A702931P301	Metal film: 10K ohms ±1%, 200 VDCW, 1/8 w.
R50	19A702931P388	Metal film: 80.6K ohms ±1%, 200 VDCW, 1/8 w.
R51 thru R53	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R54	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R55 and R56	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R57 and R58	19B800607P1	Metal film: Jumper.
R59	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R60	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R61	19A702931P413	Metal film: 133K ohms ±1%, 200 VDCW, 1/8 w.
R62	19A702931P327	Metal film: 18.7K ohms ±1%, 200 VDCW, 1/8 w.
R63	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R64	19A702931P177	Metal film: 619 ohms ±1%, 200 VDCW, 1/8 w.
R65	19B800607P682	Metal film: 6.8K ohms ±5%, 1/8 w.
R66	19A702931P243	Metal film: 2740 ohms ±1%, 200 VDCW, 1/8 w.
R67	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R68	19B800607P153	Metal film: 15K ohms ±5%, 1/8 w.
R69	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R70	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R71	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R72	19A702931P269	Metal film: 5110 ohms ±1%, 200 VDCW, 1/8 w.
R73	19A702931P313	Metal film: 13.3K ohms ±1%, 200 VDCW, 1/8 w.
R74	19B800607P561	Metal film: 560 ohms ±5%, 1/8 w.
R75 and R76	19B800607P224	Metal film: 220K ohms ±5%, 1/8 w.
R77	19A702931P376	Metal film: 60.4K ohms ±1%, 200 VDCW, 1/8 w.
R78	19A702931P222	Metal film: 1650 ohms ±1%, 200 VDCW, 1/8 w.
R80 and R81	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R82	19B800607P562	Metal film: 5.6K ohms ±5%, 1/8 w.
R83	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R84	19B800607P823	Metal film: 82K ohms ±5%, 1/8 w.
R85	19A702931P434	Metal film: 221K ohms ±1%, 200 VDCW, 1/8 w.
R86	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R87	19B800607P105	Metal film: 1M ohms ±5%, 1/8 w.
R88	19A702931P305	Metal film: 11K ohms ±1%, 200 VDCW, 1/8 w.
R89	19A702931P384	Metal film: 73.2K ohms ±1%, 200 VDCW, 1/8 w.
R90	19A702931P358	Metal film: 39.2K ohms ±1%, 200 VDCW, 1/8 w.
R91	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R92	19A702931P384	Metal film: 73.2K ohms ±1%, 200 VDCW, 1/8 w.
R93	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R94	19A702931P388	Metal film: 80.6K ohms ±1%, 200 VDCW, 1/8 w.
R95	19A702931P325	Metal film: 17.8K ohms ±1%, 200 VDCW, 1/8 w.
R96	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R97	19A702931P382	Metal film: 69.8K ohms ±1%, 200 VDCW, 1/8 w.
R98	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R99	19A702931P350	Metal film: 32.4K ohms ±1%, 200 VDCW, 1/8 w.
R100	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R101	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R102	19B800607P563	Metal film: 56K ohms ±5%, 1/8 w.
R103	19B800607P123	Metal film: 12K ohms ±5%, 1/8 w.
R104 and R105	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R106	19A702931P355	Metal film: 36.5K ohms ±1%, 200 VDCW, 1/8 w.
R107	19A702931P285	Metal film: 7500 ohms ±1%, 200 VDCW, 1/8 w.
R108	19A702931P177	Metal film: 619 ohms ±1%, 200 VDCW, 1/8 w.
R109	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R110	19B800607P105	Metal film: 1M ohms ±5%, 1/8 w.
R111	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R112 and R113	19A702931P401	Metal film: 100K ohms ±1%, 200 VDCW, 1/8 w.
R114	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R115 and R116	19B800607P391	Metal film: 390 ohms ±5%, 1/8 w.
R117	19A702931P385	Metal film: 75K ohms ±1%, 200 VDCW, 1/8 w.

*COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NO.	DESCRIPTION
R120	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R121	19A702931P342	Metal film: 26.7K ohms ±1%, 200 VDCW, 1/8 w.
R122	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R124	19A702931P325	Metal film: 17.8K ohms ±1%, 200 VDCW, 1/8 w.
R125	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R126	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R127	19A702931P401	Metal film: 100K ohms ±1%, 200 VDCW, 1/8 w.
R128 and R129	19A702931P222	Metal film: 1650 ohms ±1%, 200 VDCW, 1/8 w.
R130	19A702931P422	Metal film: 165K ohms ±1%, 200 VDCW, 1/8 w.
R132	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R133 and R134	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R135	19A702931P313	Metal film: 13.3K ohms ±1%, 200 VDCW, 1/8 w.
R136 and R137	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R138	19A702931P285	Metal film: 7500 ohms ±1%, 200 VDCW, 1/8 w.
R139	19A702931P389	Metal film: 82.5K ohms ±1%, 200 VDCW, 1/8 w.
R140	19B800607P224	Metal film: 220K ohms ±5%, 1/8 w.
R141	19A702931P269	Metal film: 5110 ohms ±1%, 200 VDCW, 1/8 w.
R142	19B800607P474	Metal film: 470K ohms ±5%, 1/8 w.
R143	19A702931P436	Metal film: 232K ohms ±1%, 200 VDCW, 1/8 w.
R144	19A702931P243	Metal film: 2740 ohms ±1%, 200 VDCW, 1/8 w.
R145	19B800607P224	Metal film: 220K ohms ±5%, 1/8 w.
R146	19B800607P474	Metal film: 470K ohms ±5%, 1/8 w.
R147	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R148	19B800607P153	Metal film: 15K ohms ±5%, 1/8 w.
R149 thru R151	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R152	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R153	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R155	19A702931P434	Metal film: 221K ohms ±1%, 200 VDCW, 1/8 w.
R156	19A702931P406	Metal film: 113K ohms ±1%, 200 VDCW, 1/8 w.
R157	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R158	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R159	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R160	19A702931P177	Metal film: 619 ohms ±1%, 200 VDCW, 1/8 w.
R161	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R162	19B800607P474	Metal film: 470K ohms ±5%, 1/8 w.
R163	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R164	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R165	19B800607P682	Metal film: 6.8K ohms ±5%, 1/8 w.
R166	19A702931P355	Metal film: 36.5K ohms ±1%, 200 VDCW, 1/8 w.
R167	19A702931P325	Metal film: 17.8K ohms ±1%, 200 VDCW, 1/8 w.
R168	19A702931P305	Metal film: 11K ohms ±1%, 200 VDCW, 1/8 w.
R169	19A702931P393	Metal film: 90.9K ohms ±1%, 200 VDCW, 1/8 w.
R170 and R171	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R172 and R173	19B800607P474	Metal film: 470K ohms ±5%, 1/8 w.
R174	19A702931P313	Metal film: 13.3K ohms ±1%, 200 VDCW, 1/8 w.
R175	19B800607P333	Metal film: 33K ohms ±5%, 1/8 w.
R176	19A702931P222	Metal film: 1650 ohms ±1%, 200 VDCW, 1/8 w.
R177	19A702931P269	Metal film: 5110 ohms ±1%, 200 VDCW, 1/8 w.
R178	19B800607P474	Metal film: 470K ohms ±5%, 1/8 w.
R179	19A702931P385	Metal film: 75K ohms ±1%, 200 VDCW, 1/8 w.
R180	19A702931P413	Metal film: 133K ohms ±1%, 200 VDCW, 1/8 w.
R181	19A702931P130	Metal film: 200 ohms ±1%, 200 VDCW, 1/8 w.
R183	19B800607P183	Metal film: 18K ohms ±5%, 1/8 w.
R184	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R185	19B800607P473	Metal film: 47K ohms ±5%, 1/8 w.
R186	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
		- - - - - - - - - - SWITCHES - - - - - - - - -
SW2 thru SW4	19A705959P3	Switch, toggle: SPDT, 0.4 A @ 20 volts; sim to C & K T101-M-H9-A-B-E.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U1	19A705982P101	Microcomputer: 8-bit extended I/O; sim to INTEL 80C152JB-1.
U2	19A703471P302	Digital: Octal Data Latch; sim to 74HC373.
U3	19A703471P320	Digital: 3-Line To 8-Line Decoder; sim to 74HC138.
U4	344A3307G13	EPROM Kit.
U5	19A705603P5	Digital: 8K x 8-Bit Static CMOS RAM; sim to KM6264AL-10
U6	19A703952P102	EEPROM: 2K X 8, 5 Volts, programmable; sim to XICOR X2816CP-20.
U7	19A704380P319	Digital: CMOS Octal Data Flip-Flop; sim to 74HC377.
U8	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U9	344A3070P3	Digital: JFET, Input quad Op Amp; sim to TL074.
U10	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U11	19A116297P7	Linear: Dual Op Amp; sim to MC4558CD.
U12	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U13	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U14	19A702705P3	Digital: 8-Channel Analog Multiplexer; sim to 4051BM.
U15	344A3856P101	CMOS Analog Multiplexer; sim to DG408D.
U16 and U17	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U18	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U19	19A149895P1	Digital: supervisory circuit; sim to MAXIM MAX691C.
U20	19A116180P575	Digital: Hex Open Collector Inverter: sim to 7406.
U21	19A703995P3	Digital: High speed logic, hex inverter, unbuffered; sim to 74HCU04.
U22	344A3039P201	Digital: Driver/receiver, EIA-232D/V.28; sim to MC145406.
U24	19A705980P101	Tranxceiver, differential Bus; sim to SN751768.
U25	19A703471P316	Digital: Driver/receiver, octal 3-state non inverting buffer; sim to 74HC541.
U26	19A116180P575	Digital: Hex Open Collector Inverter: sim to 7406.
U27	19A705979P101	Digital: CMOS A/D; sim to TL549CP.
U28	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U29	19A149466P301	Digital: CH MOS, programmable timer; sim to INTEL 82C54.
U30	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U31	344A3070P3	Digital: JFET, Input quad Op Amp; sim to TL074.
U32 and U33	19A702705P3	Digital: 8-Channel Analog Multiplexer; sim to 4051BM.
U34	19A705991P101	Digital: Programmable interface; sim to Harris C82C55A.
U35 and U36	344A3041P201	Digital: dual in-line potentiometers, ceramic, hermetically sealed; sim to DS1267S-10.
U37	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U40	19A116180P575	Digital: Hex Open Collector Inverter: sim to 7406.
U41	19A700176P101	Digital: Hex Inverting Buffer/Converter; sim to 4049UBD.
XU4	19A705840P2	Socket: sim to Amp 643646-3.
		- - - - - - - - - - CRYSTALS - - - - - - - - -
Y1	19A702511G37	Crystal Assembly: 14.7456 MHz.

SYMBOL	PART NO.	DESCRIPTION
		DIGITAL SIGNAL PROCESSOR 19D902667G1
		- - - - - - - - - - CAPACITORS - - - - - - - - -
C1 thru C15	19A702052P26	Ceramic: 0.1 µF ± 10%, 50 VDCW.
C16 and C17	19A702061P29	Ceramic: 22 pF ± 5%, 50 VDCW, temp coef 0 ± 30 PPM.
C18 thru C22	19A705205P6	Tantalum: 10 µF, 16 VDCW; sim to Sprague 293D.
C24	19A702052P107	Ceramic: 2200 pF ± 5%, 50 VDCW.
C25	19A702061P53	Ceramic: 68 pF ± 5%, 50 VDCW, temp coef 0 ± 30 PPM.
C26	19A702052P120	Ceramic: 0.033 µF ± 5%, 50 VDCW.
C27 and C28	19A705205P19	Tantalum: 2.2 µF ±20%, 10VDCW; sim to Sprague 293D.
C29	19A702052P134	Ceramic: 0.1µF ± 5%, 25
C30	19A702052P112	Ceramic: 6800 pF ± 5%, 50 VDCW.
C31	19A702052P105	Ceramic: 1000 pF ± 5%, 50 VDCW.
C32	19A702052P142	Ceramic: 0.082 µF ± 5%, 16 VDCW.
C33 and C34	19A702052P112	Ceramic: 6800 pF ± 5%, 50 VDCW.
C35	19A702052P105	Ceramic: 1000 pF ± 5%, 50 VDCW.
C38	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 + or - 30 PPM.
		- - - - - - - - - - DIODES - - - - - - - - - -
D1 and D2	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
		- - - - - - - - - - PLUGS - - - - - - - - - -
P2 and P3	19A704779P14	Connector, 15 pin.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R2	19B800607P1	Metal film: Jumper.
R4	19B800607P1	Metal film: Jumper.
R5 and R6	19B800607P683	Metal film: 68K ohms ±5%, 1/8 w.
R7	19B800607P1	Metal film: Jumper.
R10	19B800607P682	Metal film: 6.8K ohms ±5%, 1/8 w.
R12 and R13	19B800607P1	Metal film: Jumper.
R14 and R15	19A702931P355	Metal film: 36.5K ohms ±1%, 200 VDCW, 1/8
R16	19A702931P318	Metal film: 15K ohms ±1%, 200 VDCW, 1/8 w.
R17	19A702931P401	Metal film: 100K ohms ±1%, 200 VDCW, 1/8 w.
R18	19B800607P201	Metal film: 200 ohms ±5%, 1/8 w.
R20	19B800607P392	Metal film: 3.9K ohms ±5%, 1/8 w.
R21	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R23 thru R27	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R28 and R29	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R30	19A702931P418	Metal film: 150K ohms ±1%, 200 VDCW, 1/8 w.
R31	19A702931P318	Metal film: 15K ohms ±1%, 200 VDCW, 1/8 w.
R32	19A702931P209	Metal film: 1210 ohms ±1%, 200 VDCW, 1/8 w.
R33	19A702931P369	Metal film: 51.1K ohms ±1%, 200 VDCW, 1/8 w.

SYMBOL	PART NO.	DESCRIPTION
R34	19A702931P331	Metal film: 20.5K ohms ±1%, 200 VDCW, 1/8 w.
R35	19A702931P201	Metal film: 1000 ohms ±1%, 200 VDCW, 1/8 w.
R36	19A702931P317	Metal film: 14.7K ohms ±1%, 200 VDCW, 1/8 w.
R37	19A702931P331	Metal film: 20.5K ohms ±1%, 200 VDCW, 1/8 w.
R38	19A702931P377	Metal film: 61.9K ohms ±1%, 200 VDCW, 1/8 w.
R39	19A702931P307	Metal film: 11.5K ohms ±1%, 200 VDCW, 1/8 w.
R40	19A702931P347	Metal film: 30.1K ohms ±1%, 200 VDCW, 1/8 w.
R41 and R42	19A702931P157	Metal film: 383 ohms ±1%, 200 VDCW, 1/8 w.
R43	19A702931P339	Metal film: 24.9K ohms ±1%, 200 VDCW, 1/8 w.
R44	19A702931P347	Metal film: 30.1K ohms ±1%, 200 VDCW, 1/8 w.
R45	19A702931P307	Metal film: 11.5K ohms ±1%, 200 VDCW, 1/8 w.
R46	19A702931P294	Metal film: 9310 ohms ±1%, 200 VDCW, 1/8 w.
R47	19A702931P265	Metal film: 4640 ohms ±1%, 200 VDCW, 1/8 w.
R48	19A702931P294	Metal film: 9310 ohms ±1%, 200 VDCW, 1/8 w.
R49 thru R51	19A702931P201	Metal film: 1000 ohms ±1%, 200 VDCW, 1/8 w.
R55	19A702931P301	Metal film: 10K ohms ±1%, 200 VDCW, 1/8 w.
R56	19A702931P339	Metal film: 24.9K ohms ±1%, 200 VDCW, 1/8 w.
R57	19A702931P301	Metal film: 10K ohms ±1%, 200 VDCW, 1/8 w.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U1	344A3038P101	Digital: DSP microcomputer, oper freq. 40.96 MHz; sim to ADSP210KX-40.
U4 and U5	19A705827P1	Encoder/Decoder: sim to Texas Instruments TCM29C23.
U6	344A3309G5	EPROM Kit.
U7	344A3064P203	Digital: HI-SPEED, octal D type FF, pos. edge trig.; sim to 74HCT377.
U8	344A3064P201	Digital: HI-SPEED, 3-8 line decoder/demultiplexer, inverting; sim to 74HCT138.
U9	344A3064P204	Digital: HI-SPEED, octal buffer/line driver, 3-state; sim to 74HCT541
U10	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U11	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U12	344A3040P201	Digital: SRAM, 1K X 8 Dual port; sim to IDT7130SA100.
U13	344A3064P202	Digital: HI-SPEED, transparent ltch, 3-state; sim to 74HCT373.
U15	344A3041P201	Digital: dual in-line potentiometers, ceramic, hermetically sealed; sim to DS1267S-10.
U16	344A3070P3	Digital: JFET, Input quad Op Amp; sim to TL074.
U17	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U18	344A3070P3	Digital: JFET, Input quad Op Amp; sim to TL074.
		- - - - - - - - - - SOCKETS - - - - - - - - - -
X1	19A702511G30	Crystal, quartz: 8.192 MHz.
		- - - - - - - - - - SOCKETS - - - - - - - - - -
XU1	19B235688P1	Socket,PLCC
XU6	19A705840P2	Socket: sim to Amp 643646-3.

PRODUCTION CHANGES

Changes to the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by those revisions.

System Module - 19D902590G2

To standardize production of MASTR IIe and MASTR III System Modules, changed MASTR IIe System Board from 19D902453G1 to 19D902771G1.

MASTR IIe System Board was: 19D902453G1 (see LBI-38639 for a description of this board).

System Board - 19D902771G1

Rev. A: To improve operation, changed R57 from 19B800607P472 (4.7K ohms) to 19A702931P305 (11k ohms).

Rev. B: To make MASTR IIe and MASTR III System Boards compatible, changed R127 from 19A702931P269 (5.11K ohms) to 19A702931P401 (100K ohms).

Rev. C: To enhance audio routing by supplying CAS in the System Module in auxiliary receiver applications. Changed the following resistors:

Changed R24 from 19B800607P822 (8.2K ohms) to 19B800607P272 (2.7K ohms).

Changed R57 from 19B702931P305 (11K ohms) to 19B8800607P1 (Jumper).

Changed R82 from 19B800607P103 (19K ohms) to 19B800607P562 (5.6K ohms).

Rev. D: To improve performance, changed R24 from 19B800607P272 (2.7K ohms) to 19B800607P122 (1.2K ohms).

Rev. E: In order to meet the 10% variance of the complete audio path. Changed the following capacitors:
Changed C79 from 19A702052P14 (±10%) to 19A702052P114 (±5%).
Changed C103 from 19A702052P14 (±10%) to 19A702052P114 (±5%).

Digital Signal Processor - 19D902667G1

Rev. A-C: Incorporated into initial shipment.

Rev. D: To invert SYSBD Line in to accommodate 2-wire line audio cancellation, added C36-C38, D2, R50-R54, R56, R57, and U18. Changed C29 and deleted R155.

C29 was: 19A702052P26, 0.1 µF 10%, 50 VDCW.

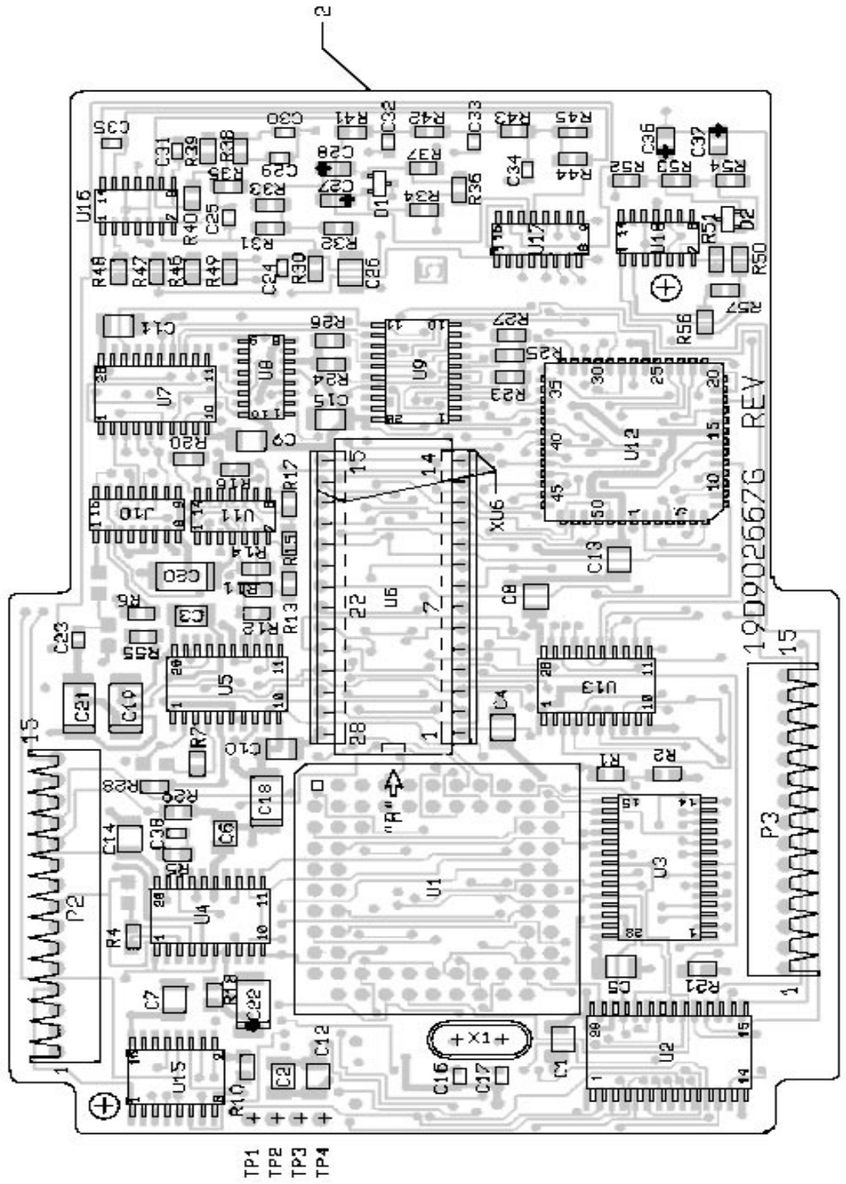
Rev. E: To adjust analog signal levels to protect hardware from excessive signal levels, changed R50, R51, and R53 and Deleted U2 and U3.

Changed R50 from 19A702931P265 (4640 ohms) to 19A702931P201 (1.0K ohms).

Changed R51 from 19A702931P265 (4640 ohms) to 19A702931P201 (1.0K ohms).

Changed R53 from 19A702931P305 (11K ohms) to 19A702931P265 (4640 ohms).

COMPONENT SIDE

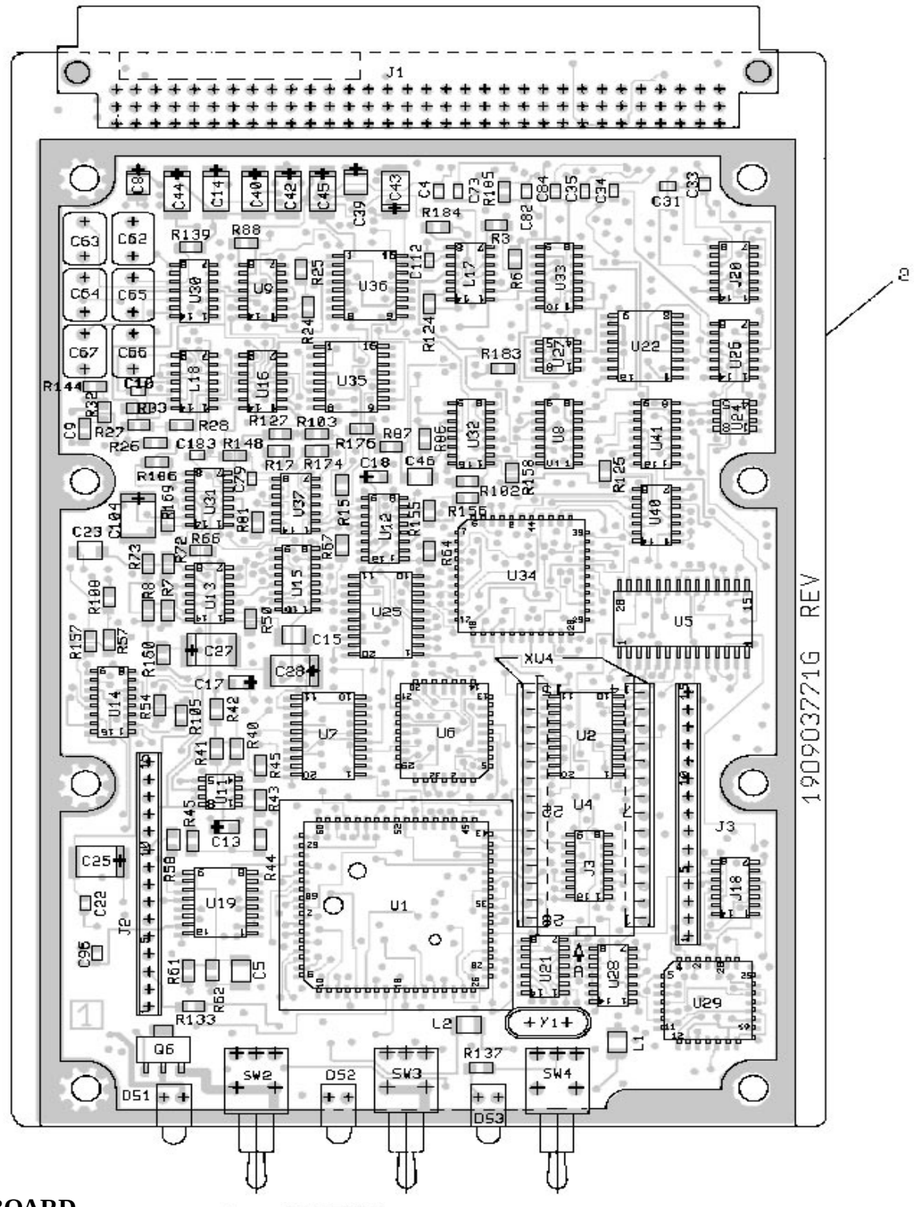


CAUTION
OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

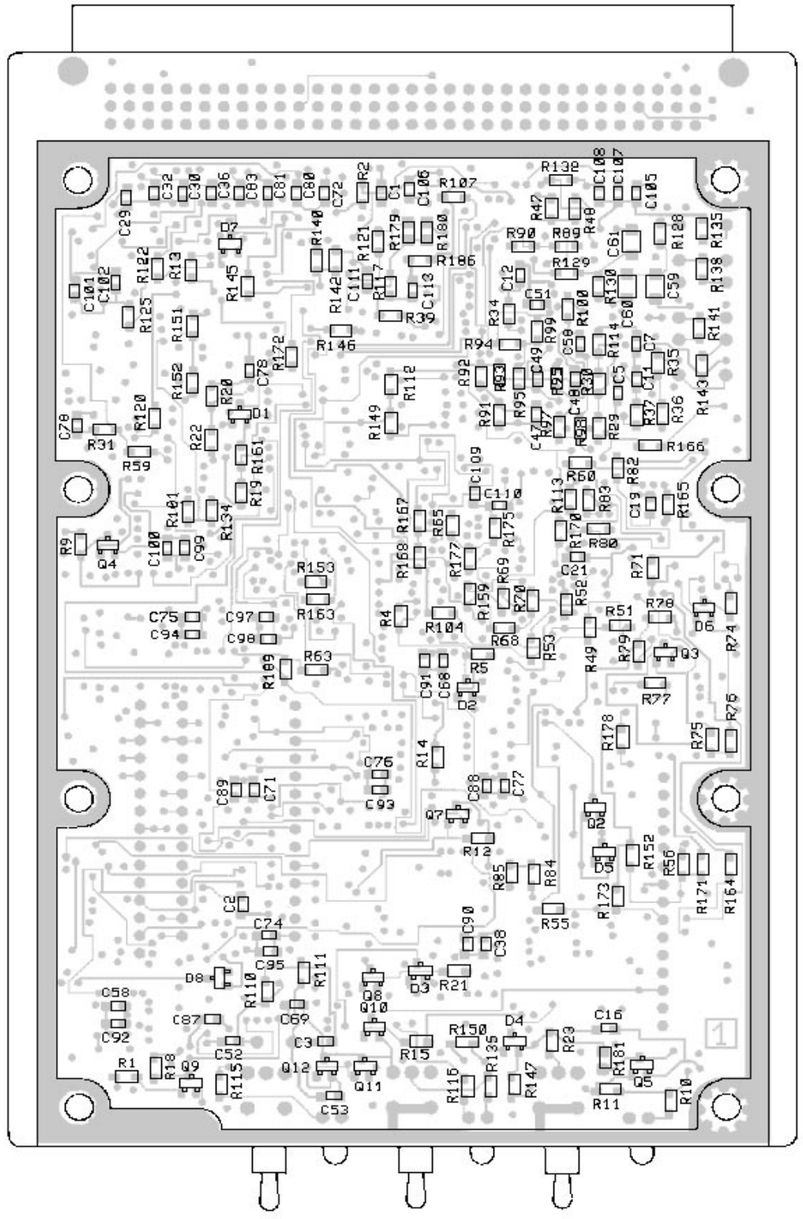
DSP BOARD 19D902667G1

(19D902667, Sh. 1, Rev. 5)
(19D902668, Layer 1, Rev. 5)

COMPONENT SIDE



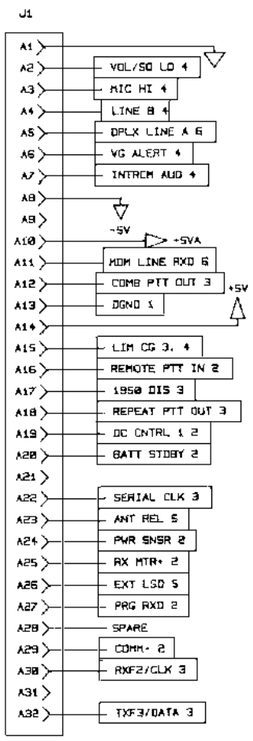
SOLDER SIDE

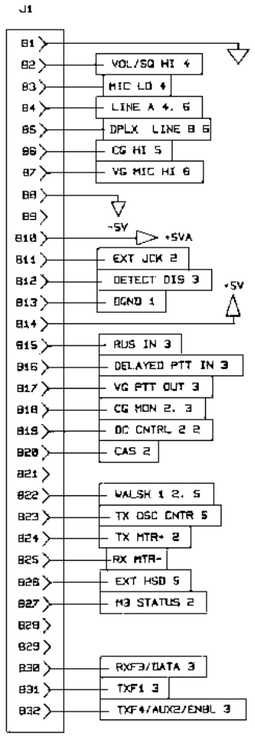


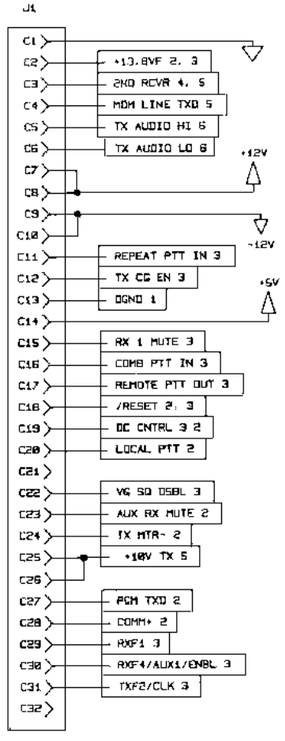
SYSTEM BOARD
19D903771G1

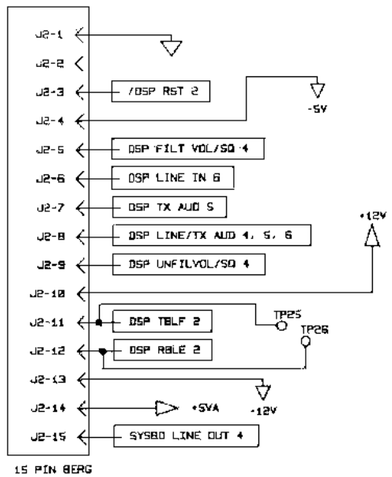
(19D903771, Sh. 1, Rev. 2)
(19D903772, Layer 1, Rev. 1A)
(19D903772, Layer 6, Rev. 1A)

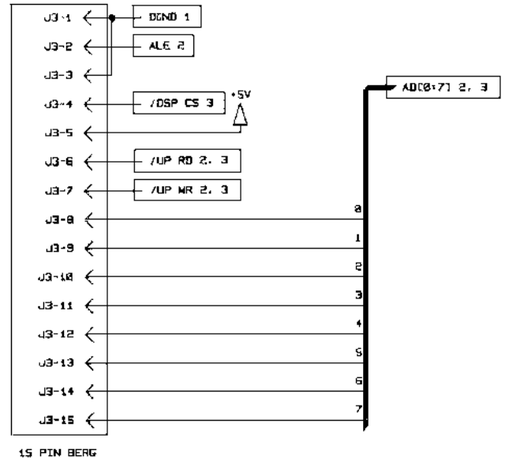
CAUTION
OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES

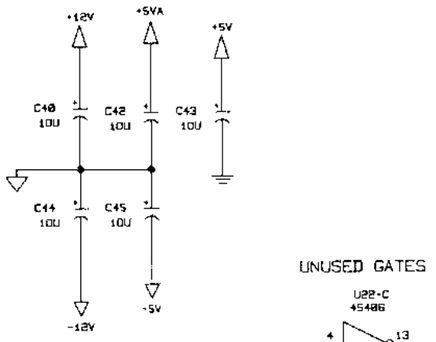


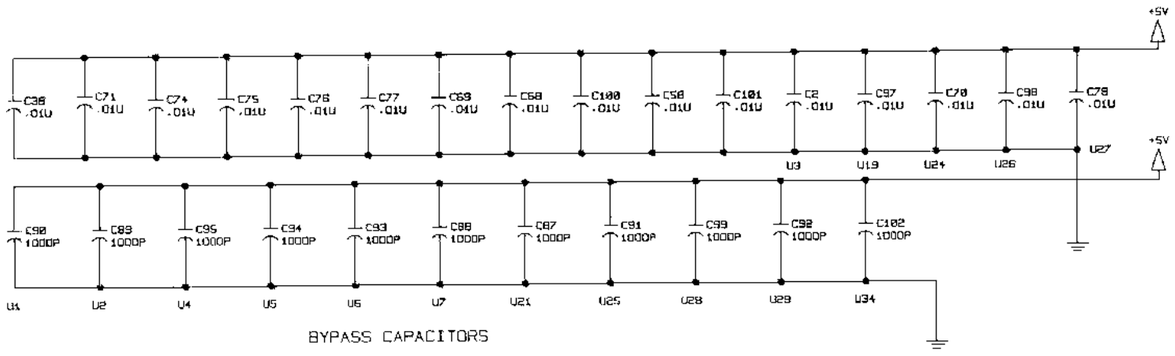


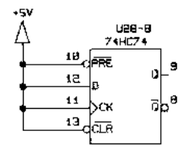




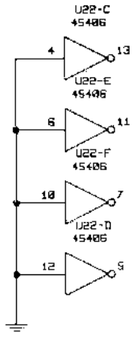








UNUSED GATES

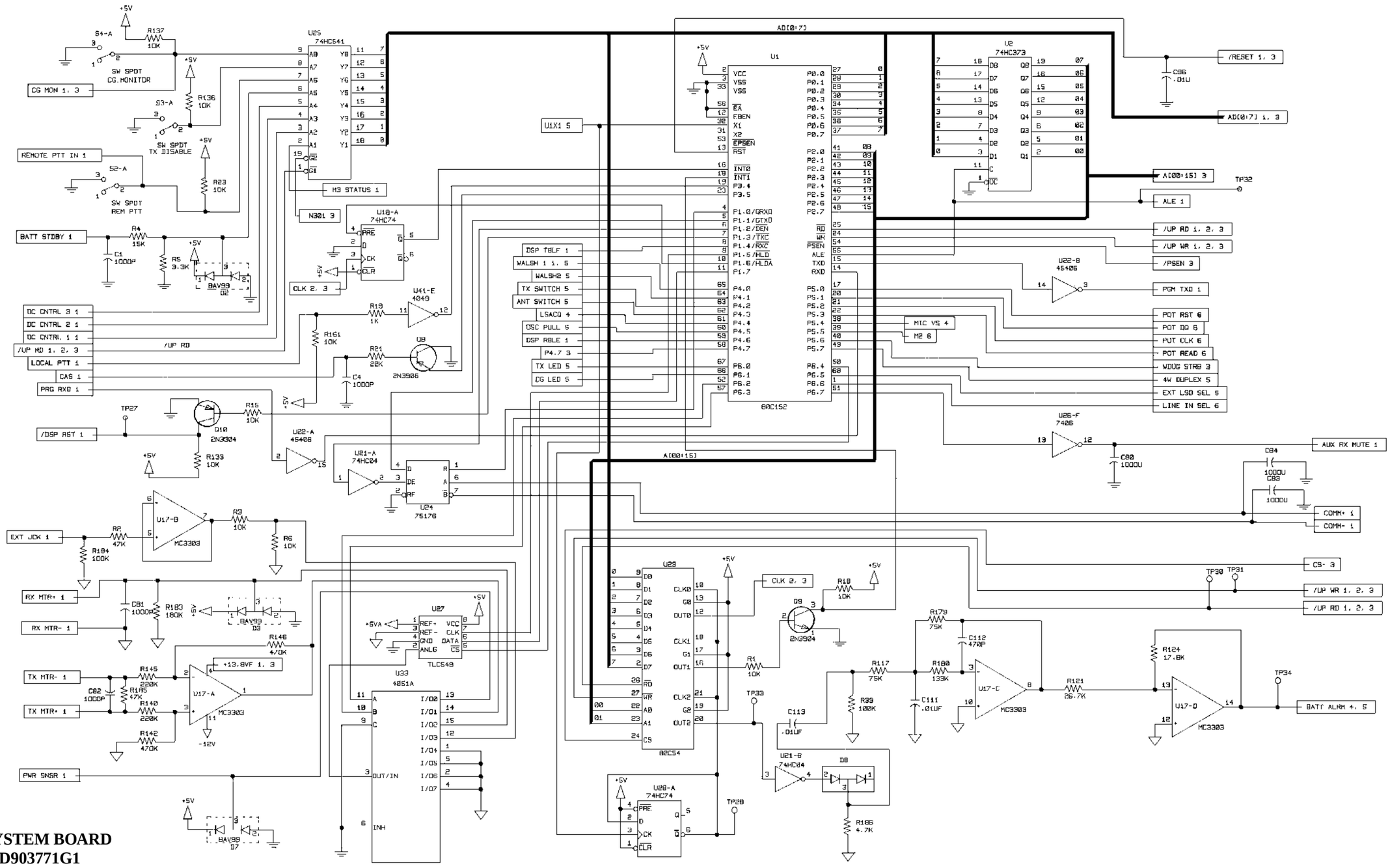


THIS SCHEMATIC DIAG APPLIES TO	
MODEL NO.	REV LETTER
PLI9D903771G1	E

ALL RESISTORS ARE 0.1 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY MULTIPLIER K OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U, N OR P
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER M OR U

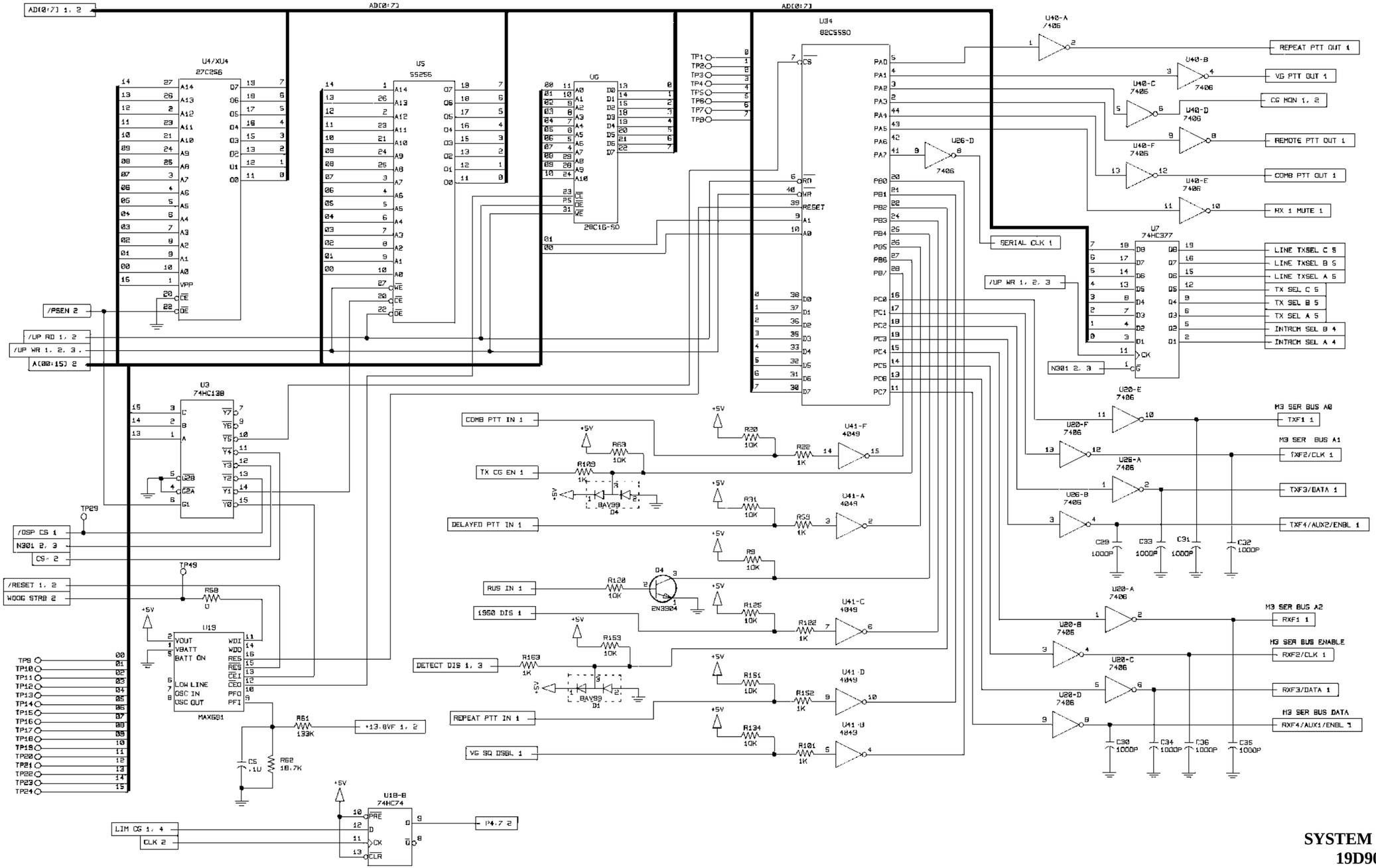
SYSTEM BOARD
19D903771G1

(19D903770, Sh. 1, Rev. 7)



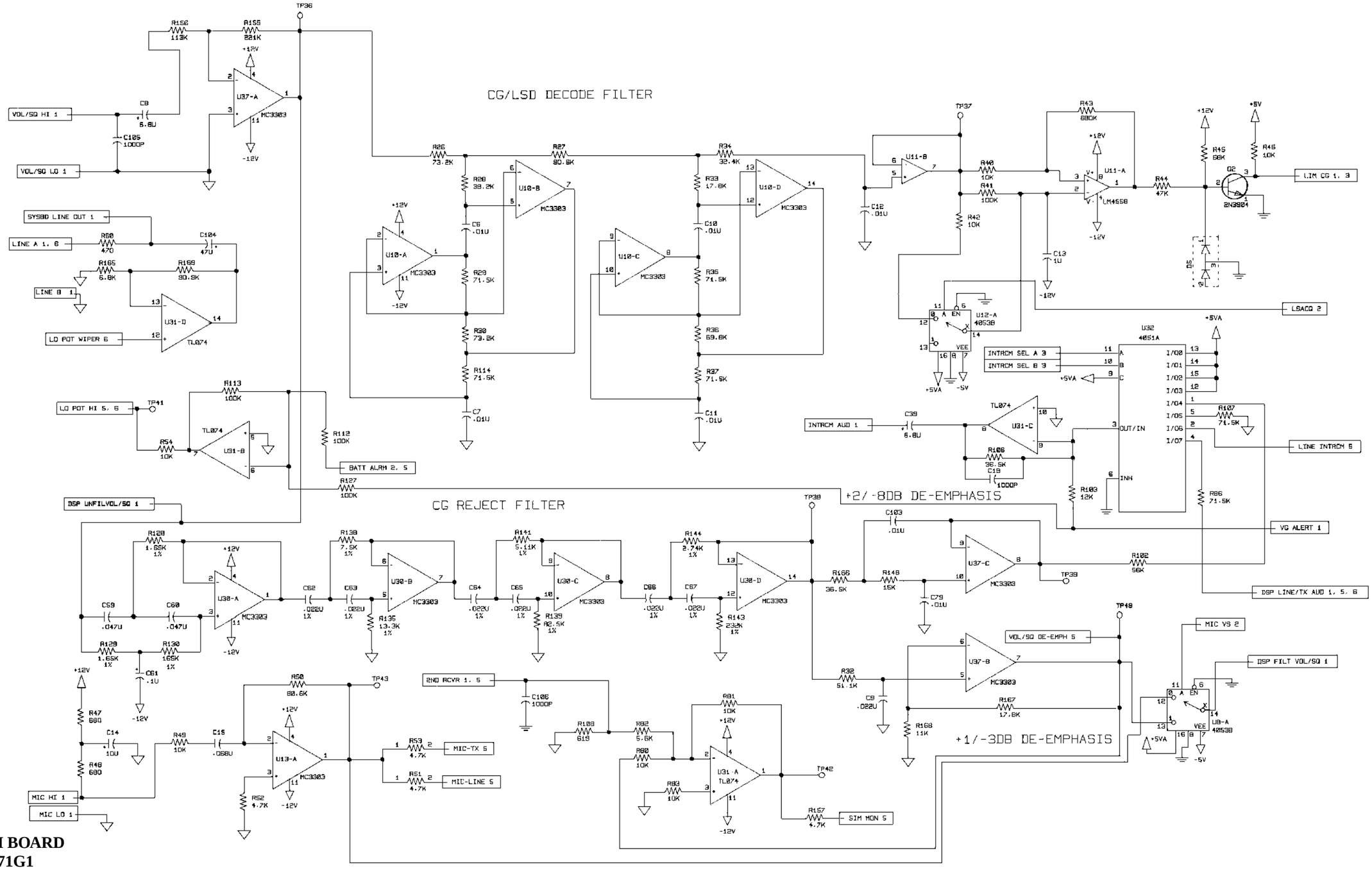
SYSTEM BOARD
19D903771G1

(19D903770, Sh. 2, Rev. 2)



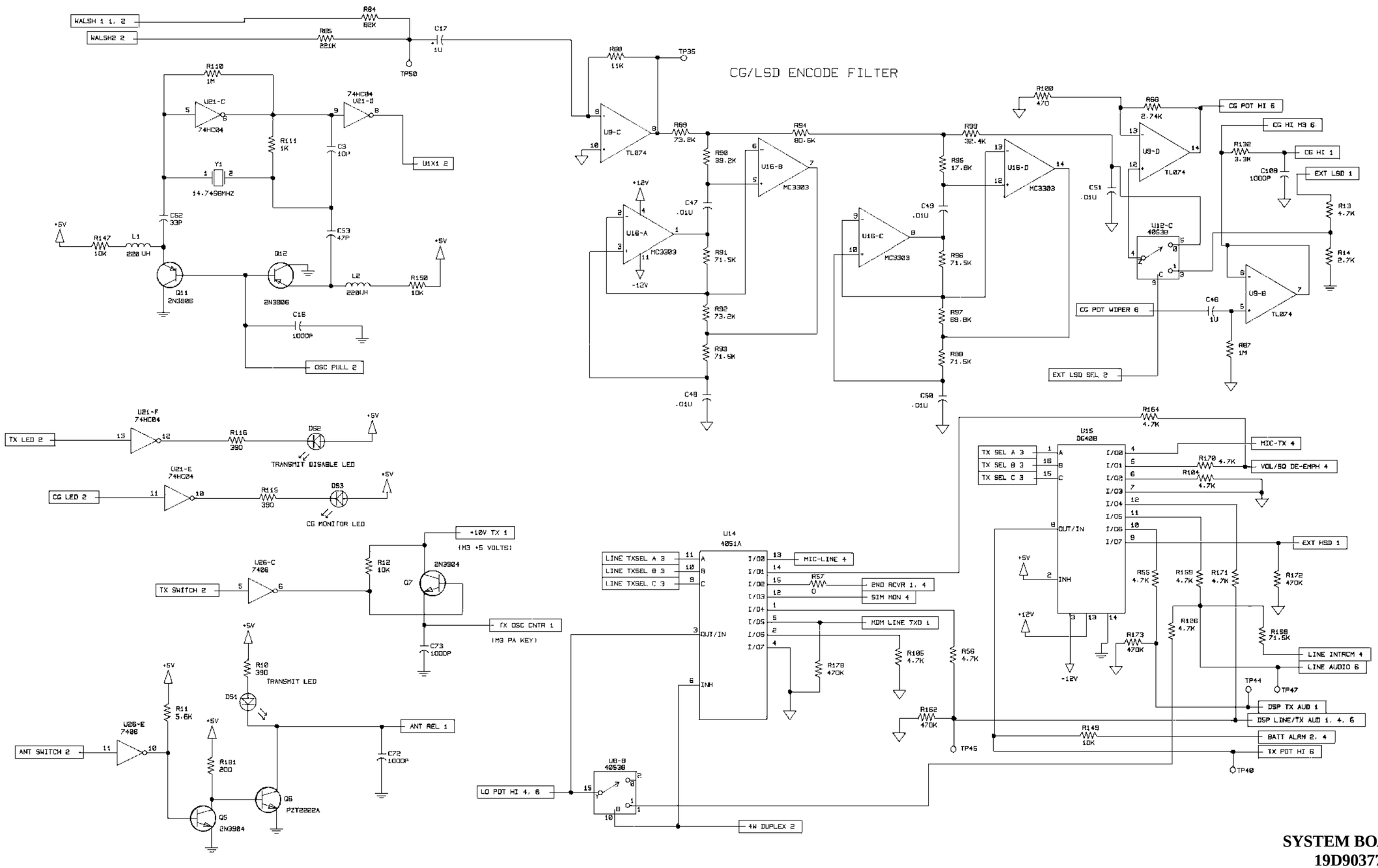
SYSTEM BOARD
19D903771G1

(19D903770, Sh. 3, Rev. 1)



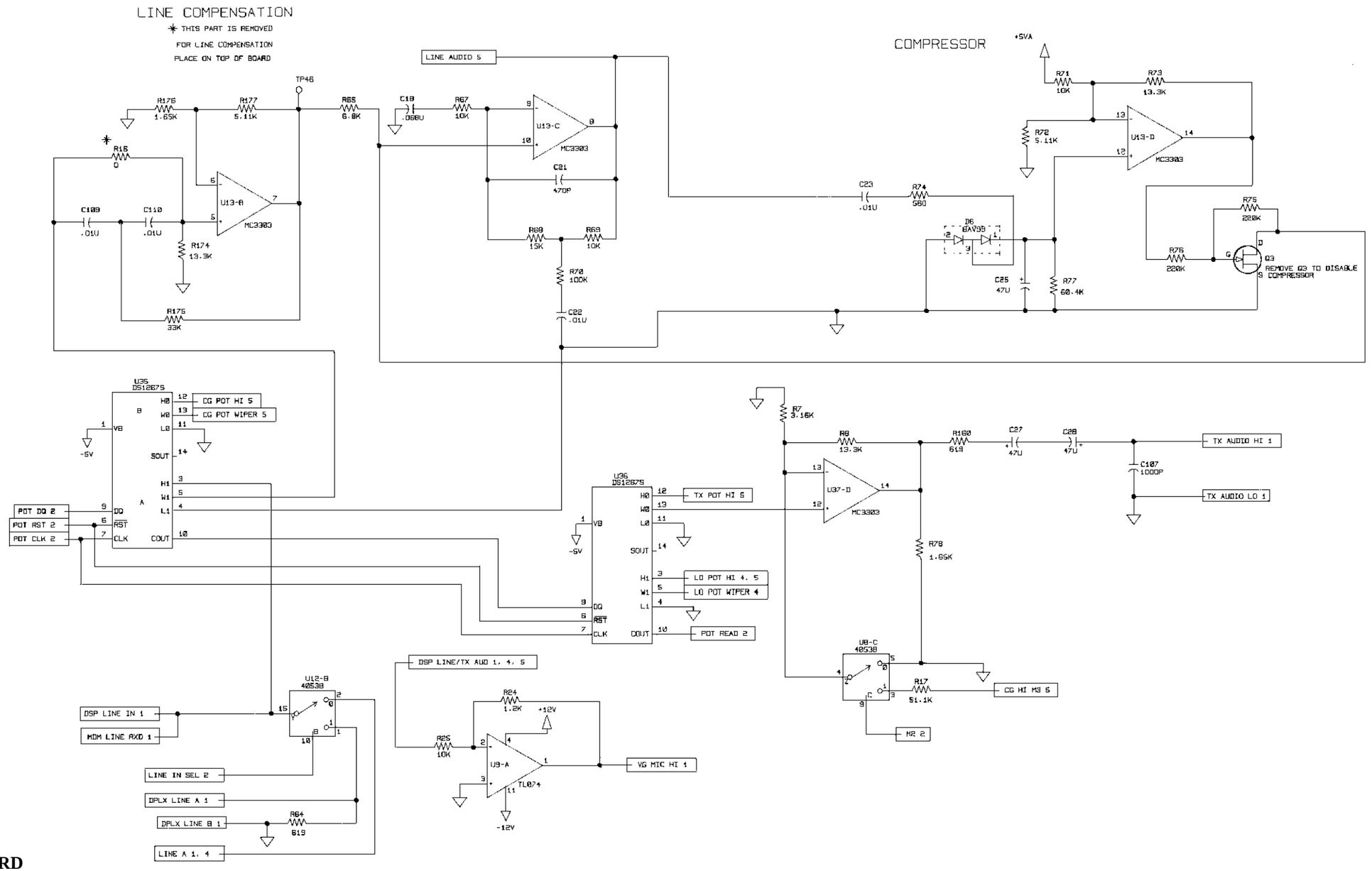
SYSTEM BOARD
19D903771G1

(19D903770, Sh. 4, Rev. 3)



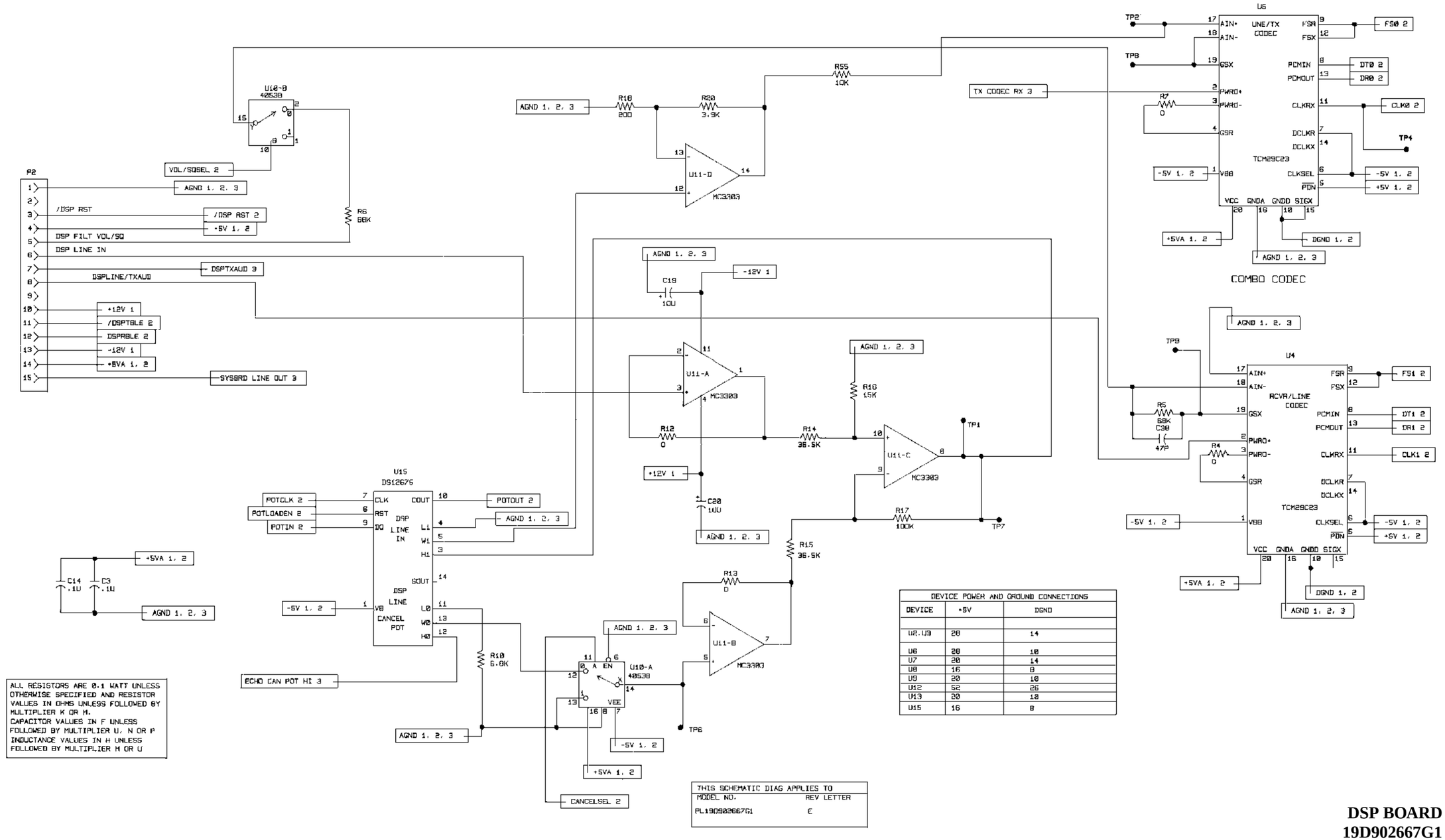
SYSTEM BOARD
19D903771G1

(19D903770, Sh. 5, Rev. 3)



SYSTEM BOARD
19D903771G1

(19D903770, Sh. 6, Rev. 3)



ALL RESISTORS ARE 0.1 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY MULTIPLIER K OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U, N OR P
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER M OR U

DEVICE POWER AND GROUND CONNECTIONS

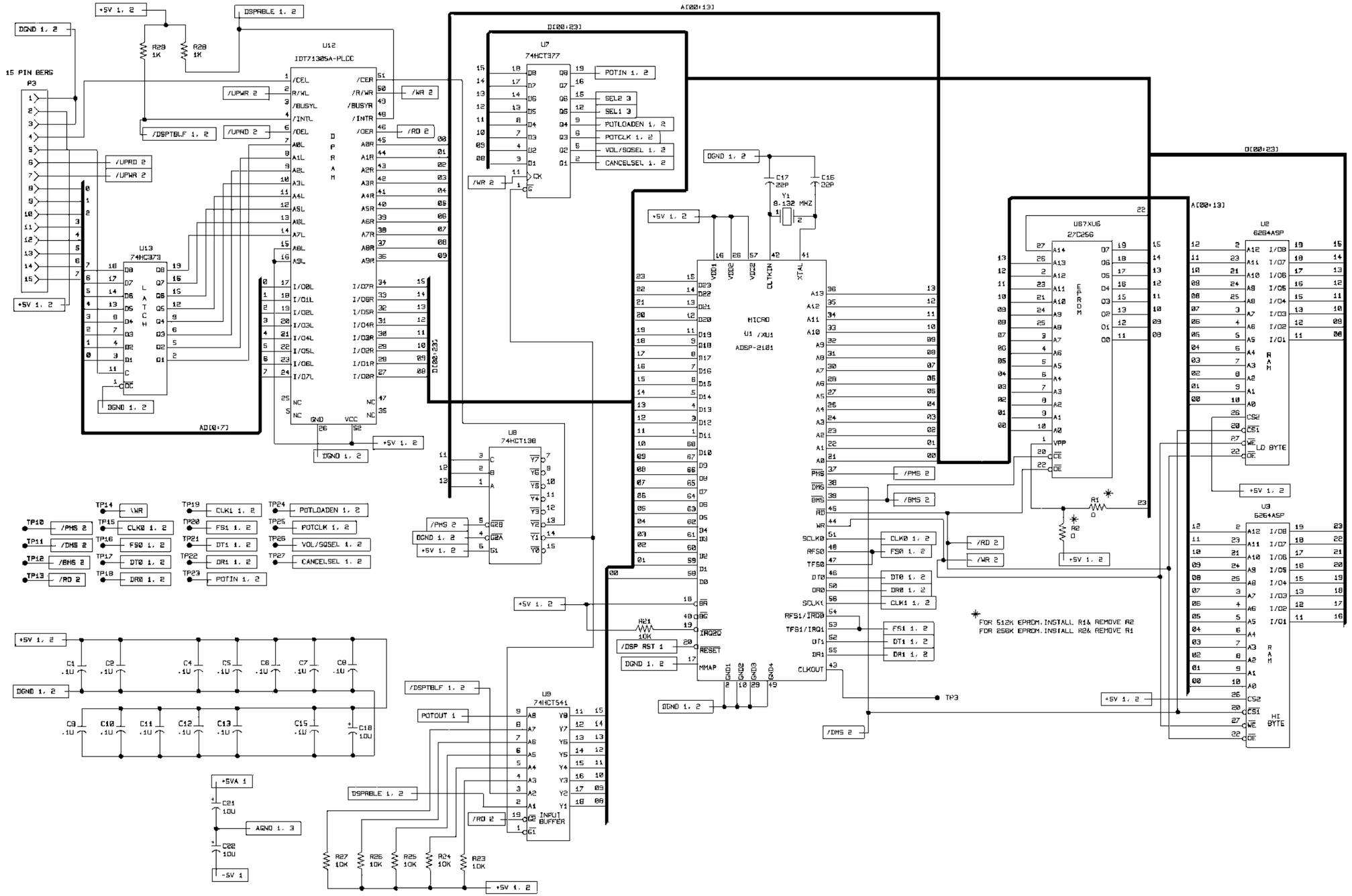
DEVICE	+5V	DGND
U2,U3	28	14
U6	20	10
U7	20	14
U8	16	8
U9	20	10
U12	52	26
U13	20	10
U15	16	8

THIS SCHEMATIC DIAG APPLIES TO

MODEL NO.	REV LETTER
PL19D902667G1	E

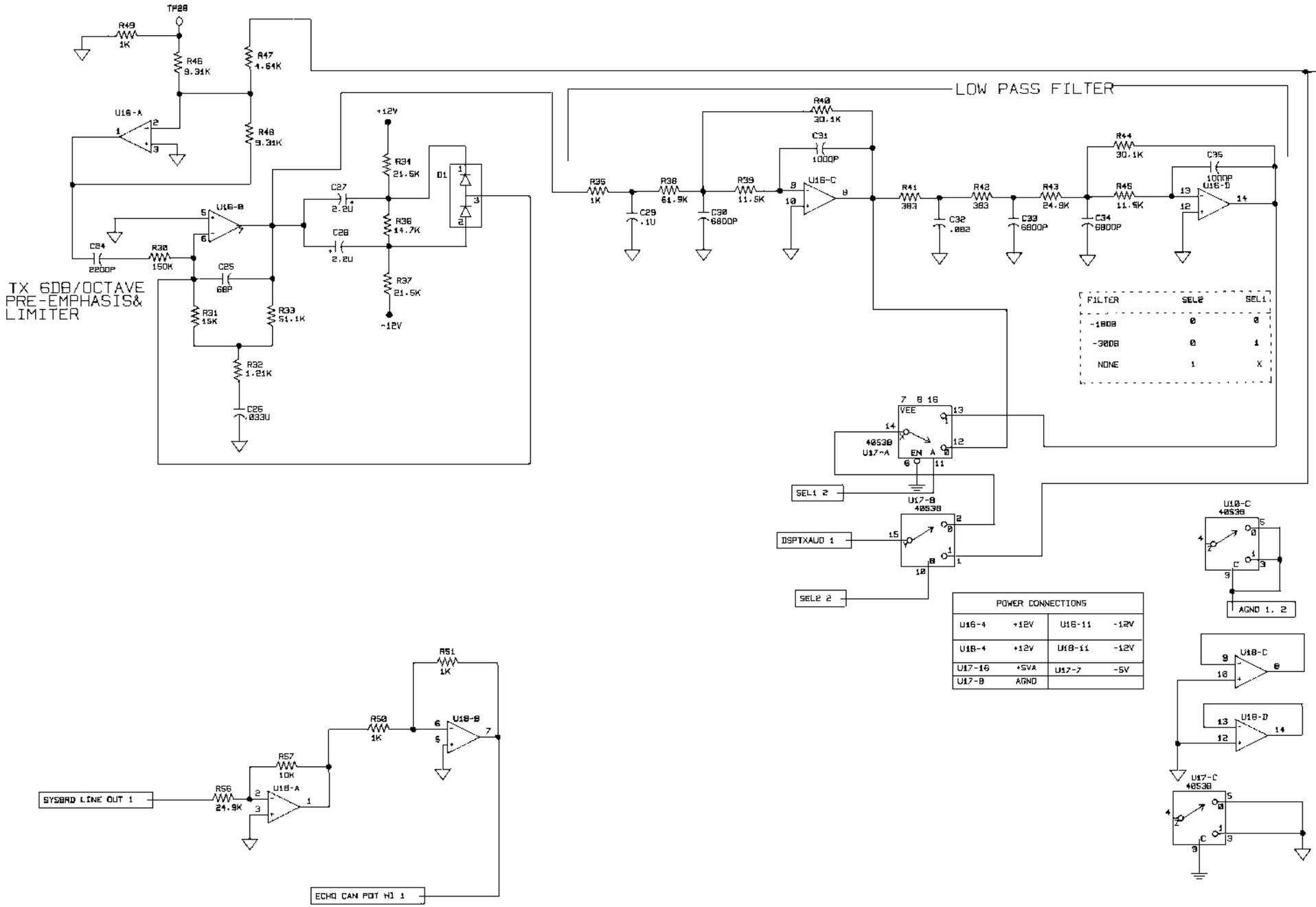
DSP BOARD
19D902667G1

(19D902910, Sh. 1, Rev. 9)



DSP BOARD
19D902667G1

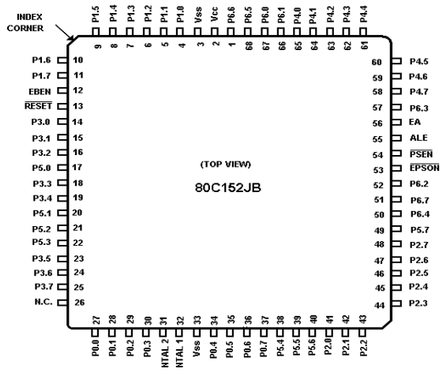
(19D902910, Sh. 2, Rev. 3)



DSP BOARD
19D902667G1

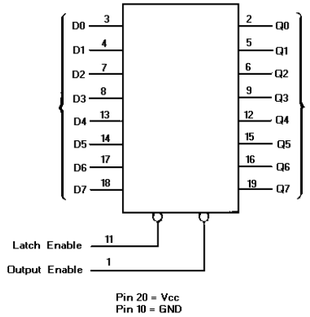
(19D902910, Sh. 3, Rev. 7)

U1, Microcomputer
19A705982P101



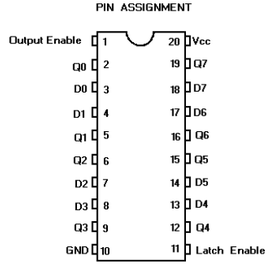
U2, Octal Data Latch
19A703471P302

BLOCK DIAGRAM



Pin 20 = Vcc
Pin 10 = GND

PIN ASSIGNMENT

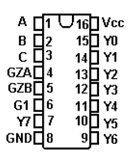


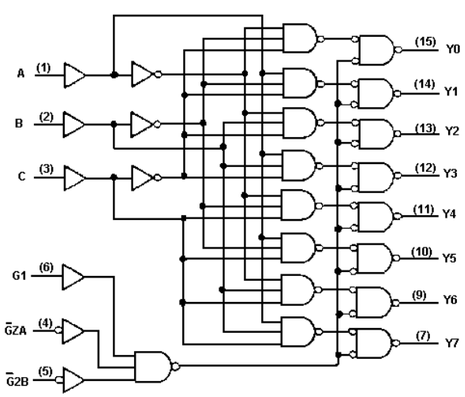
FUNCTION TABLE

Output Enable	Latch Enable	D	Output
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

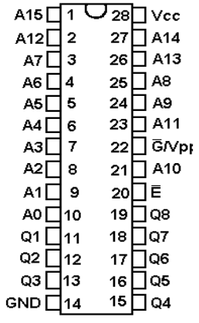
U3, 19A703471P120
3-to-8 Decoder/Demultiplexer



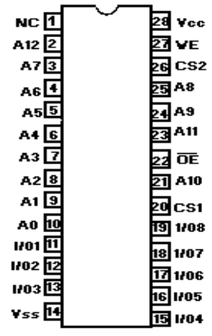


SYSTEM MODULE

U4, EPROM Kit
344A3307G5



PIN ARRANGEMENT



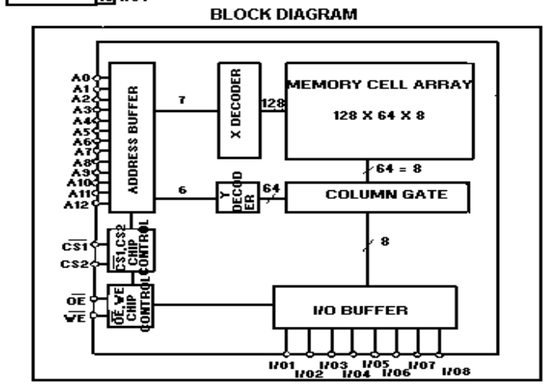
U5, 8K x 8-Bit Static CMOS RAM
19A705603P5

TRUTH TABLE

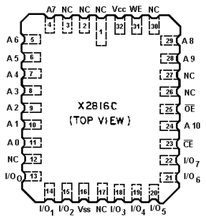
WE	CS	CS	OE	MODE	I/O PIN
X	H	X	X	NOT SELECTED (POWER DOWN)	HIGH Z
X	X	L	X		HIGH Z
H	L	H	H	OUTPUT DISABLED	HIGH Z
H	L	H	L	READ	DOUT
L	L	H	H	WRITE	D IN
L	L	H	L		D IN

X=HORL

BLOCK DIAGRAM

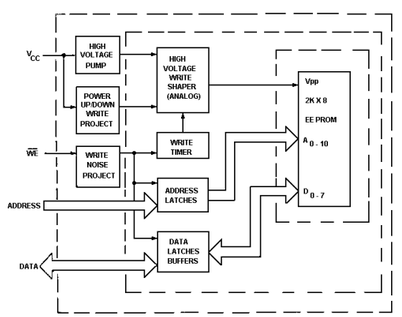


U6, Optoisolator
19A703952P102

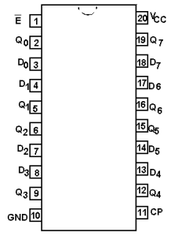


PIN NAMES

A 0 - A 10	ADDRESS INPUTS
I/O_0 - I/O_7	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
Vcc	+5V
VxX	GROUND
NC	NO CONNECT



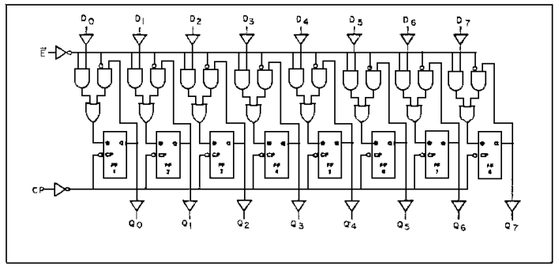
U7, CMOS Octal Data Flip-Flop
19A704380P319



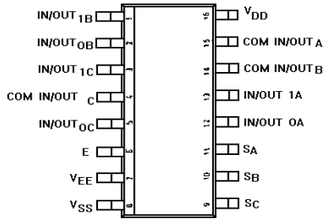
FUNCTION TABLE

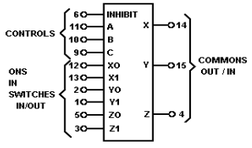
OPERATING MODES	INPUTS			OUTPUTS
	CP	Ē	D_n	Q_n
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = don't care



U8 and U12, Triple 2-Channel Analog Multiplexer
19A702705P5



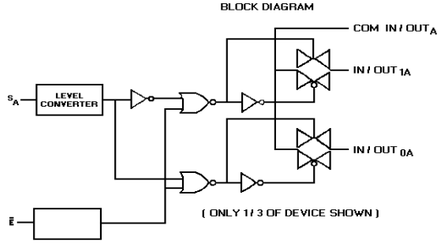


TRUTH TABLE

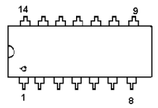
CONTROL INPUTS				ON-SWITCHES		
	SELECT					
INHIBIT	C	B	A			
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	NONE		

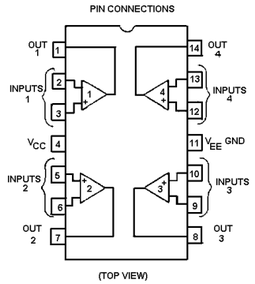
X = DON'T CARE

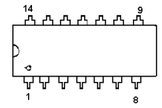
BLOCK DIAGRAM

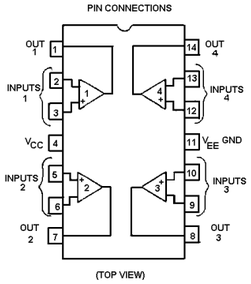


U9 and U31, Operational Amplifier
344A3070P3
U10, U13, U16, U17, U30, & U37
19A704883P2

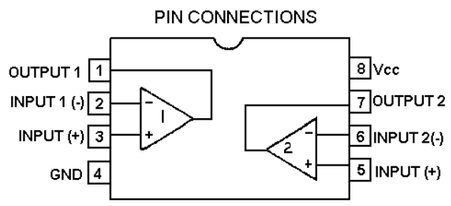




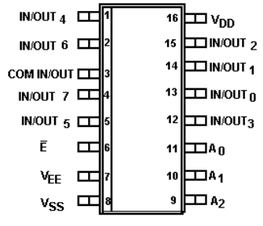


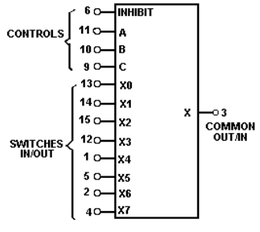


U11, Daul Op Amp
19A116297P7

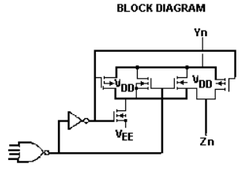


U14, U32, & U33, 8-Channel Analog Multiplexer
19A702705P3





BLOCK DIAGRAM



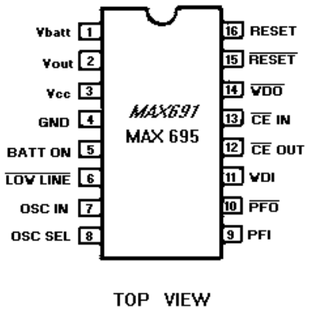
(ONLY 1/8 OF DEVICE SHOWN)

CONTROL INPUTS		
INHIBIT	SELECT	ON-SWITCHES
	C B A	
0	0 0 0	X0
0	0 0 1	X1
0	0 1 0	X2
0	0 1 1	X3
0	1 0 0	X4
0	1 0 1	X5
0	1 1 0	X6
0	1 1 1	X7
1	X X X	NONE

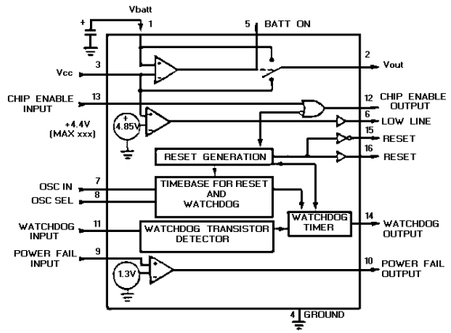
X = DON'T CARE

SYSTEM MODULE

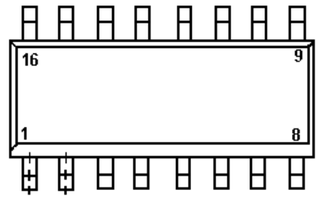
U19, Supervisory Circuit
19A149895P1



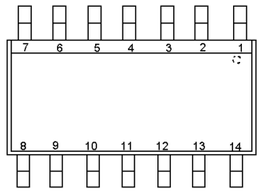
TOP VIEW

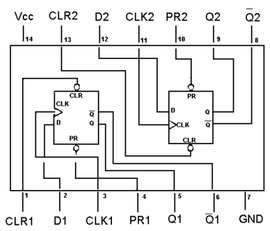


U20, U26, & U40, Hex Open Collector Inverter
19A116180P575



U18 and U28, CMOS Dual Data Flip-Flop
19A704380P302



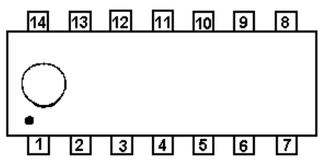


INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
K	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

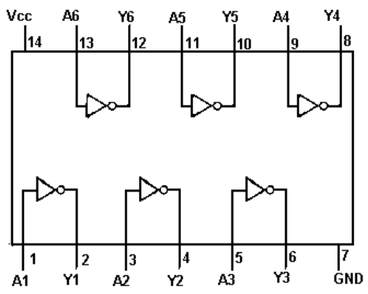
NOTE: Q0 = the level of Q before the indicated inout conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

U21, IC
19A703995P3

PIN CONFIGURATION

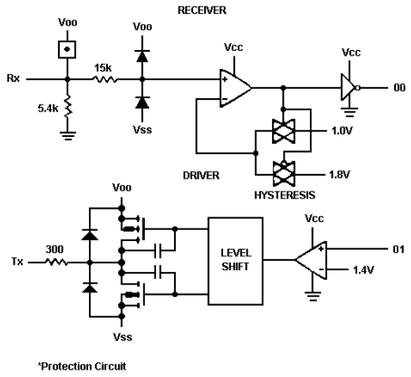


LOGIC DIAGRAM

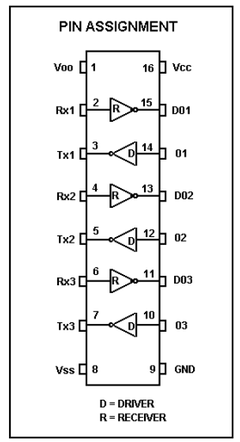


U22, Driver/Receiver: EIA-232D/V.28
344A3039P201

FUNCTION DIAGRAM



*Protection Circuit



U24, Differential Bus Transceiver
19A705980P101

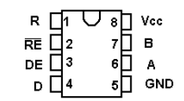
FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

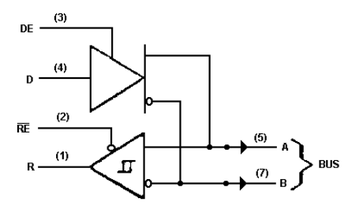
FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS A - B	ENABLE $\overline{RE}$	OUTPUT R
V_{ID} > 0.2V	L	H
-0.2V < V_{ID} < 0.2V	L	?
V_{ID} < -0.2V	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate.
X = irrelevant, z = high impedance (off)

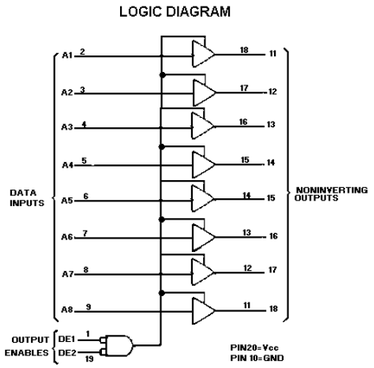


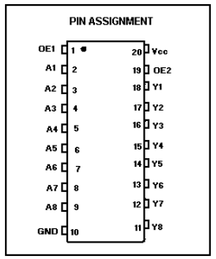
logic diagram (positive logic)



SYSTEM MODULE

U25, Octal Tri-State Transceiver
19A703471P116



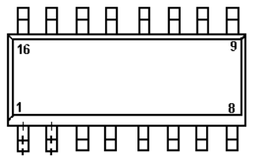


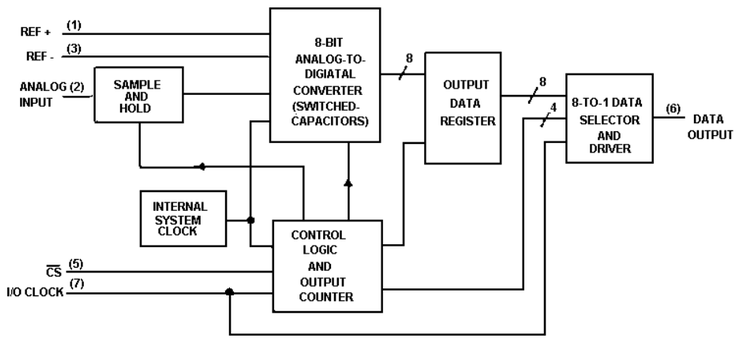
FUNCTION TABLE

INPUTS			OUTPUTS
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

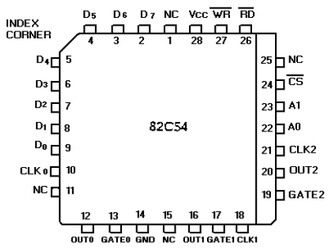
Z= high impedance
X=don't care

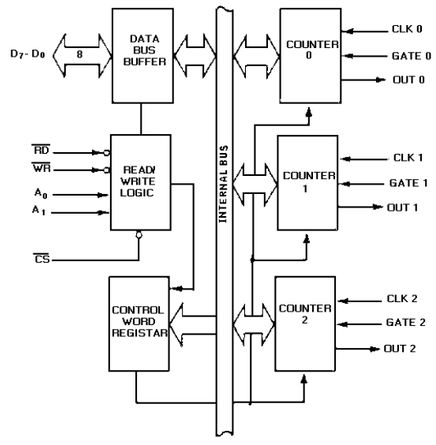
U27, CMOS A/D Converter
19A705979P101



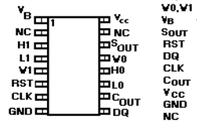


U29,CH MOS Programmable Interval Timer
19A149466P301



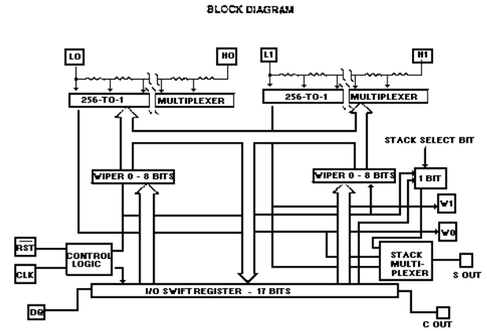


U35 and U36, Digital Potentiometer
344A3041P201

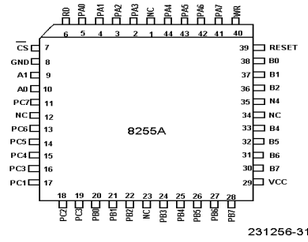


PIN NAMES

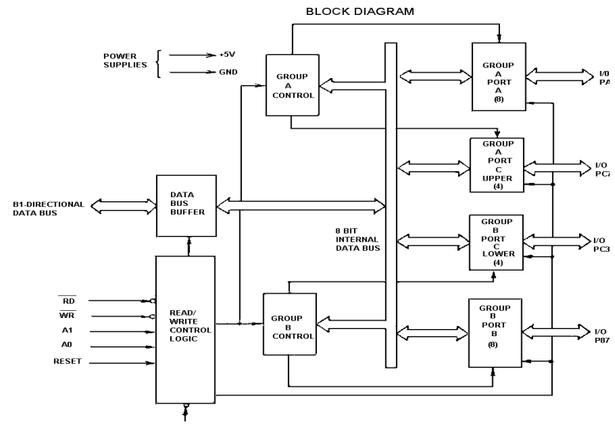
LO,L1	-	LOWER END OF RESISTOR
H0,H1	-	HIGHER END OF RESISTOR
V0,V1	-	WIPER END OF RESISTOR
V_B	-	SUBSTRATE BIAS
S_{OUT}	-	WIPER FOR STACKED CONFIGURATION
RST	-	SERIAL PORT RESET INPUT
DQ	-	SERIAL PORT DATA INPUT/OUTPUT
CLK	-	SERIAL PORT CLOCK INPUT
C_{OUT}	-	CASCADE SERAIL PORT OUTPUT
V_{CC}	-	+5 VOLT INPUT
GND	-	GROUND
NC	-	NO CONNECTION



U34, CH MOS Programmable Peripheral Interface
19A705991P101

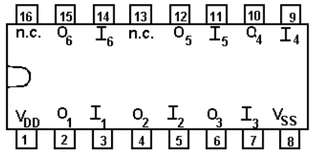


231256-31

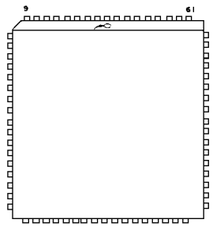


SYSTEM MODULE

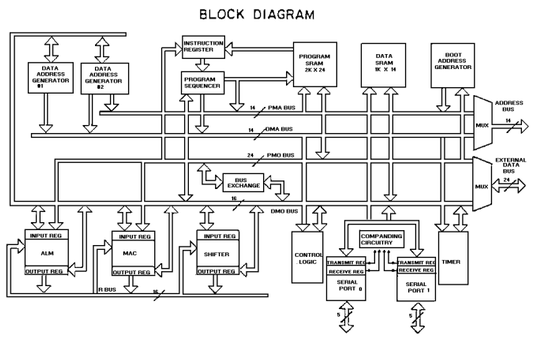
U41, Hex Inverting Buffer/Converter
19A700176P101



U1, Digital Signal Processor
344A3038P101

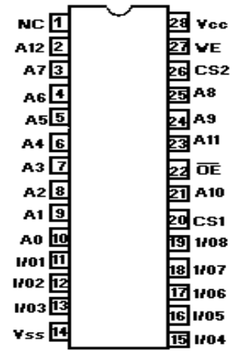


PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
B1	GND	K11	WR
B2	D19	K10	RD
C1	D20	J11	D18
C2	D21	J10	TFS0
D1	D22	H11	RFS0
D2	D23	H10	GND
E1	Vpp	G11	DR0
E2	MMAP	G10	SCLK0
F1	BR	F11	DT1
F2	TRST	F10	TFS1
G1	RESET	E11	RFS1
G2	A0	E10	DR1
H1	A1	D11	SCLK1
H2	A2	D10	VDD
J1	A3	C11	D0
J2	A4	C10	D1
K1	VDD	B11	D2
L2	A5	A10	D3
K2	A6	B10	D4
L3	GND	A9	D5
K3	A7	B9	D6
L4	A8	A8	D7
K4	A9	B8	D8
L5	A10	A7	D9
K5	A11	B7	D10
L6	A12	A6	D11
K6	A13	B6	GND
L7	PMS	A5	D12
K7	DMS	B5	D13
L8	IOS	A4	D14
K8	BG	B4	D15
L9	XTAL	A3	D16
K9	CLKIN	B3	D17
L10	CLKOUT	A2	D18
C3	Index		



U2 and U3, 8K x 8-Bit Static CMOS RAM
19A705603P5

PIN ARRANGEMENT

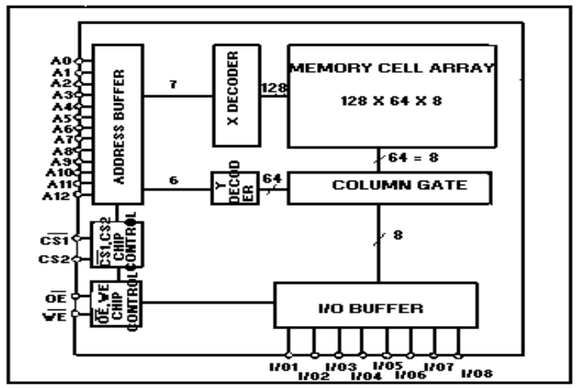


TRUTH TABLE

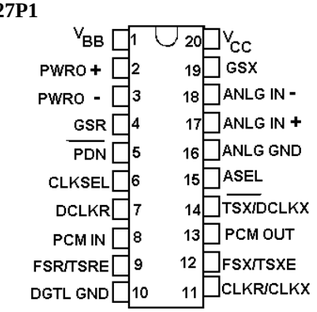
WE	CS	CS	OE	MODE	I/O PIN
X	H	X	X	NOT SELECTED (POWER DOWN)	HIGH Z
X	X	L	X		HIGH Z
H	L	H	H	OUTPUT DISABLED	HIGH Z
H	L	H	L	READ	DOUT
L	L	H	H	WRITE	D IN
L	L	H	L		D IN

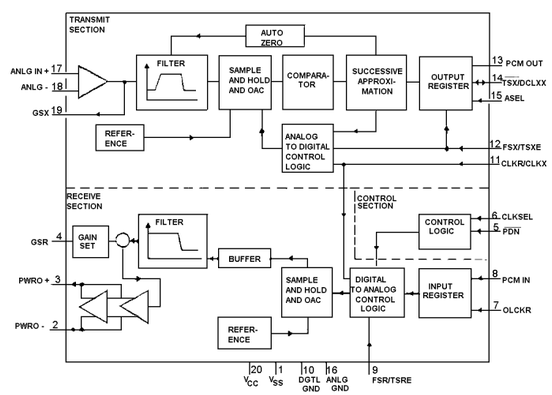
X=HORL

BLOCK DIAGRAM



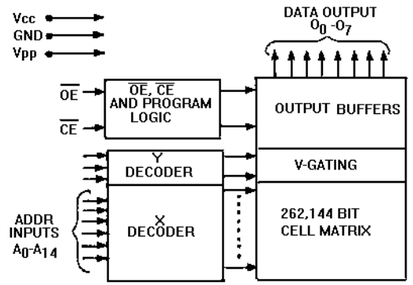
U4 and U5, Encoder/Decoder
19A705827P1

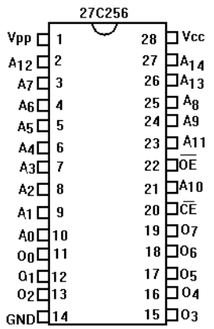




DSP BOARD

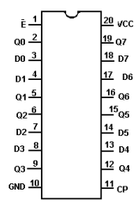
U6, EPROM Kit
344A3309G5





PIN NAME	
A_0 - A_{14}	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

U7, CMOS Hi-Speed Octal D Type Flip-Flop With Data Enable
344A3064P203

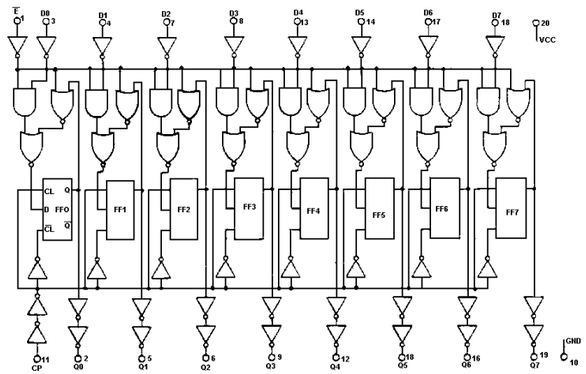


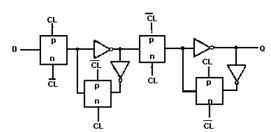
TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	E	Dn	On
LOAD "1"	⌐	l	h	H
LOAD "0"	⌐	l	X	L
HOLD (do nothing)	⌐	h	X	no change no change

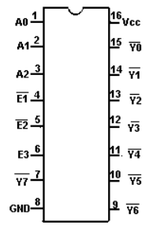
H= HIGH Voltage level steady state.
h= HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L= LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to - HIGH clock transition
X = Don't care
⌐ = LOW to -HIGH clock

BLOCK DIAGRAM





U8, CMOS Hi-Speed 3 To 8 Line Decoder/Demultiplexer
344A3064P201

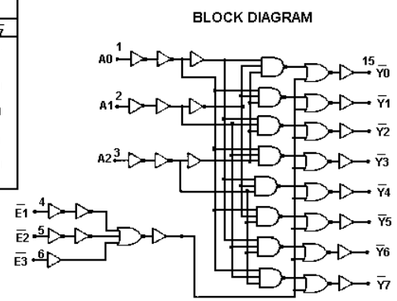


TRUTH TABLE

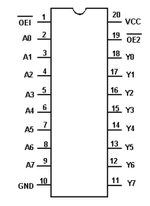
INPUTS						OUTPUTS							
ENABLE			ADDRESS										
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH LEVEL. L= LOW LEVEL. X = DON' T CARE

BLOCK DIAGRAM



U9, CMOS Hi-Speed Octal Buffer/Line Driver, 3 State
344A3064P204

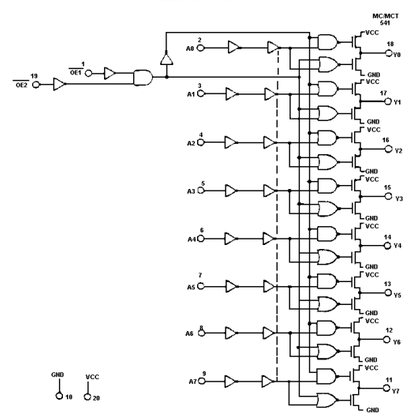


TRUTH TABLE

INPUTS			OUTPUTS
OE1	OE2	An	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

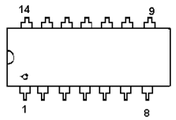
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

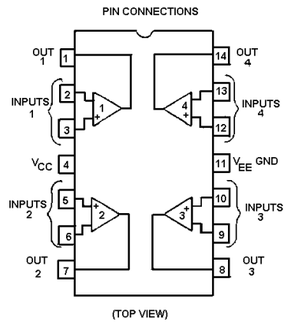
BLOCK DIAGRAM



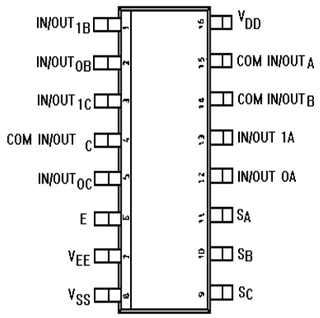
DSP BOARD

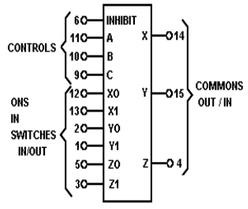
U11, Quad Operational Amplifier
19A7048883P2





U10, Triple 2-Channel Analog Multiplexer
19A702705P5



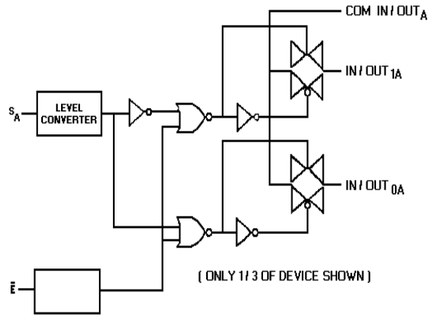


TRUTH TABLE

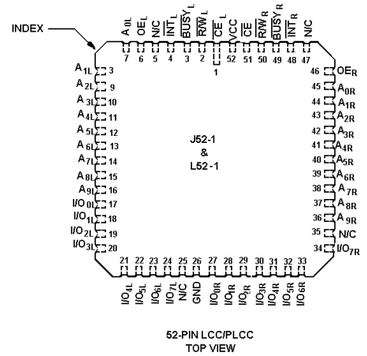
CONTROL INPUTS				ON-SWITCHES	
	SELECT				
INHIBIT	C	B	A		
0	0	0	0	Z0	Y0 X0
0	0	0	1	Z0	Y0 X1
0	0	1	0	Z0	Y1 X0
0	0	1	1	Z0	Y1 X1
0	1	0	0	Z1	Y0 X0
0	1	0	1	Z1	Y0 X1
0	1	1	0	Z1	Y1 X0
0	1	1	1	Z1	Y1 X1
1	x	x	x	NONE	

X = DON'T CARE

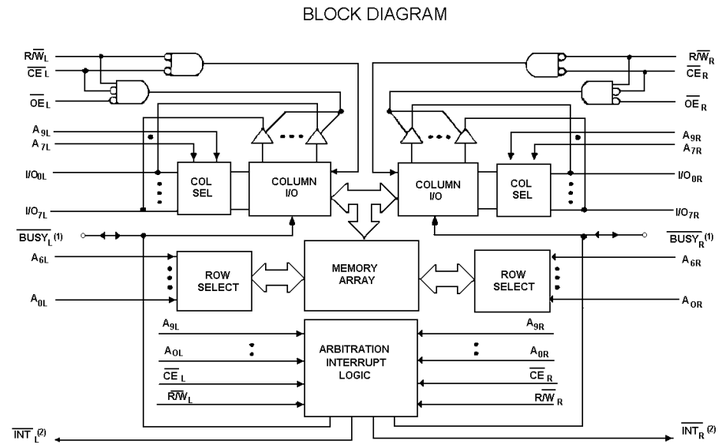
BLOCK DIAGRAM



U12, SRAM, 1K x 8, Dual Port
344A3040P201



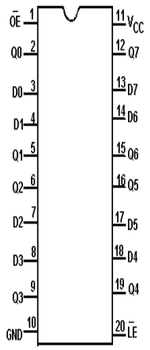
BLOCK DIAGRAM



NOTES:
1. IDT7130 (MASTER): BUSY IS OPEN DRAIN OUTPUT AND REQUIRES PULLUP RESISTOR. IDT7140(SLAVE): BUSY IS INPUT.
2. OPEN DRAIN OUTPUT REQUIRES PULLUP RESISTOR.

DSP BOARD

U13, CMOS Hi-Speed Octal Transparent Latch
344A3064P202

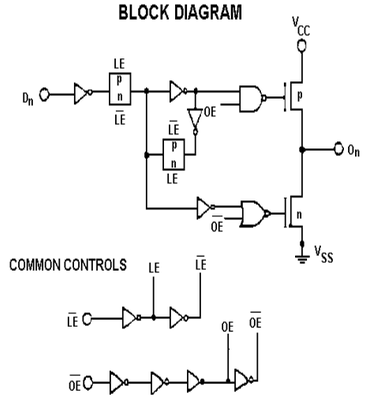


TRUTH TABLE

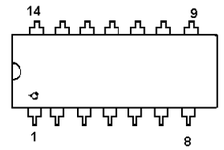
OUTPUT ENABLE	LATCH ENABLE	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

NOTE:
L = Low voltage level
H = High voltage level
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition.
X = Don't care
Z = High impedance state

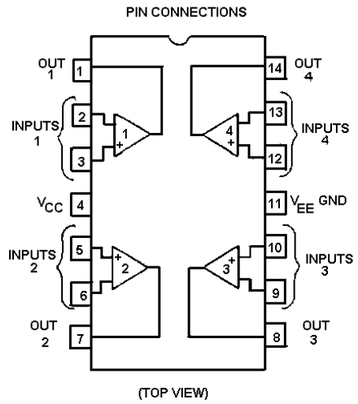
BLOCK DIAGRAM



U16, Operational Amplifier
344A3070P3

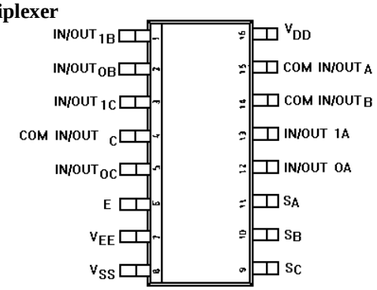


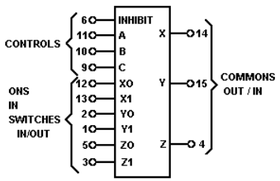
PIN CONNECTIONS



(TOP VIEW)

U17, Triple 2-Channel Analog Multiplexer
19A702705P5





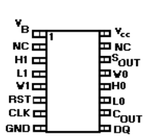
TRUTH TABLE

CONTROL INPUTS				ON-SWITCHES		
	SELECT					
INHIBIT	C	B	A			
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	NONE		

X = DON'T CARE

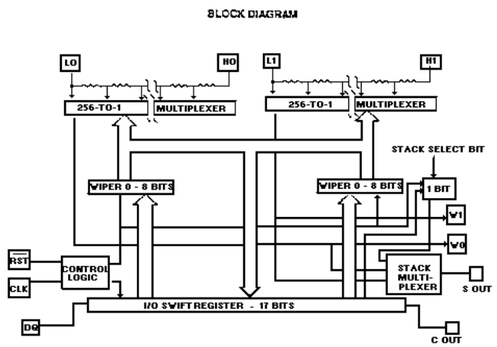
U15, Digital Potentiometer
344A3041P201

PIN NAMES

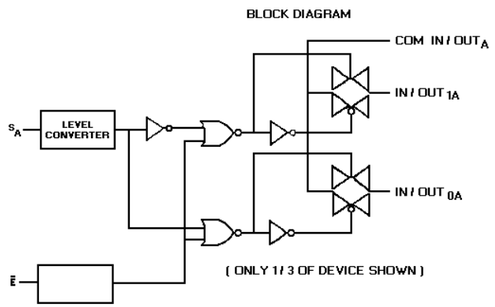


LO,L1 - LOWER END OF RESISTOR
H0,H1 - HIGHER END OF RESISTOR
W0,W1 - WIPER END OF RESISTOR
VB - SUBSTRATE BIAS
SOUT - WIPER FOR STACKED CONFIGURATION
RST - SERIAL PORT RESET INPUT
DQ - SERIAL PORT DATA INPUT/OUTPUT
CLK - SERIAL PORT CLOCK INPUT
COUT - CASCADE SERAIL PORT OUTPUT
VCC - +5 VOLT INPUT
GND - GROUND
NC - NO CONNECTION

BLOCK DIAGRAM



BLOCK DIAGRAM



(ONLY 1/ 3 OF DEVICE SHOWN)

DSP BOARD