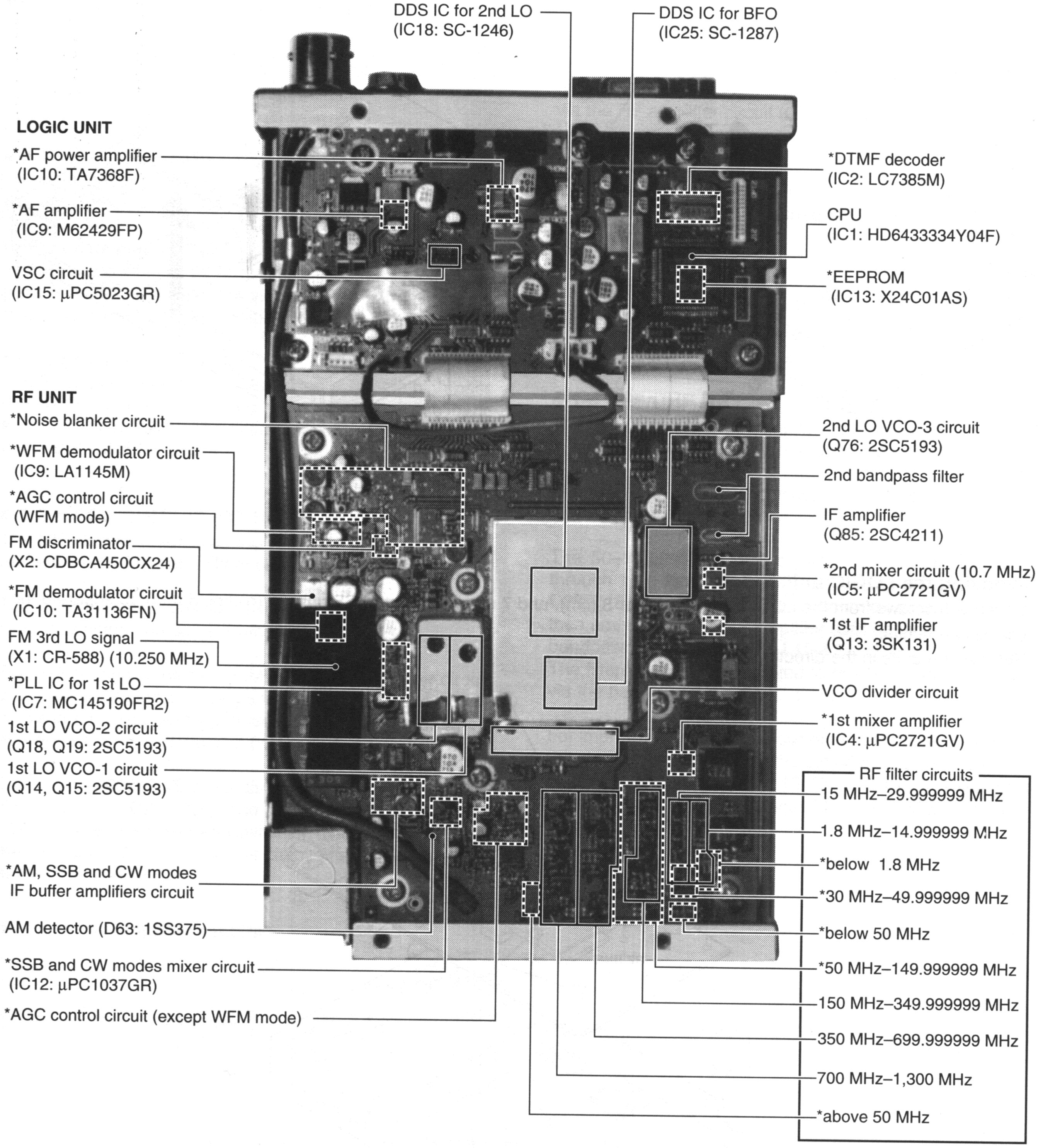
• LOGIC UNIT and RF UNIT

* : Located underside of this point.



4-1 RECEIVER CIRCUITS

4-1-1 RF ATTENUATOR CIRCUIT (RF UNIT)

The attenuator circuit attenuates the signal strength to approx. 20 dB to protect the RF amplifier from distortion when excessively strong signals are received.

The RF signals from the antenna connector are passed through or bypass the "L" type attenuator (R1, R3). The signals are then applied to the RF filter circuit.

4-1-2 RF FILTER CIRCUIT (RF UNIT)

The applied signals pass through either the low-pass filter or the high-pass filter circuits via the band switching diodes.

• RF signals below 50 MHz

The RF signals below 50 MHz are passed through the low-pass filter (L1, L2, C7–C11) via the band switching diode (D2). The filtered signals are applied to the HF RF circuit.

• RF signals above 50 MHz

The RF signals above 50 MHz are applied to the high-pass filter (L172, C651, C652) after passing through the band switching diode (D84). The filtered signals are then applied to the VHF/UHF RF circuit.

4-1-3 HF RF CIRCUIT (RF UNIT)

The HF RF circuit amplifies the received signals within the range 0.01–50 MHz and filters out-of-band signals.

The HF RF circuit consists of three low-pass filters, three high-pass filters and one RF amplifier.

The filtered signals below 1.8 MHz from the RF filter circuit are passed through the low-pass filter (L3, L4, C14– C16) between the band swithing diodes (D6, D36), and are then applied to the 1st mixer circuit (IC4).

The 1.8–14.999999 MHz signals pass through the low-pass filter (L6, L7, C21–C25) and high-pass filter (L8, L9, C26–C30) between the band switching diodes (D3, D7), and are then applied to the 1st mixer circuit after being amplified at the RF amplifier (Q12).

The 15–29.999999 MHz signals pass through the low-pass filter (L10, L11, C33–C37) and high-pass filter (L11, L12, C38–C42) between the band switching diodes (D3, D7), and are then applied to the 1st mixer circuit via the RF amplifier circuit (Q12).

The 30–49.999999 MHz signals pass through the high-pass filter (L14, L15, C45–C49) between the band switching diodes (D8, D5), and are then applied to the 1st mixer circuit via the RF amplifier circuit (Q12).

• Filters

Receive freq. (MHz)	SW diode	Filter select signal	Components
0.01–1.799999	D6, D36	B0	L3–L5, C14–C17
1.8–14.999999	D3, D7	B1	L6–L9, C21–C30
15.0–29.999999	D3, D7	B2	L10–L13, C33–C42
30.0–49.999999	D8, D5	B3	L14, L15, C45–C49

4-1-4 VHF/UHF RF CIRCUIT (RF UNIT)

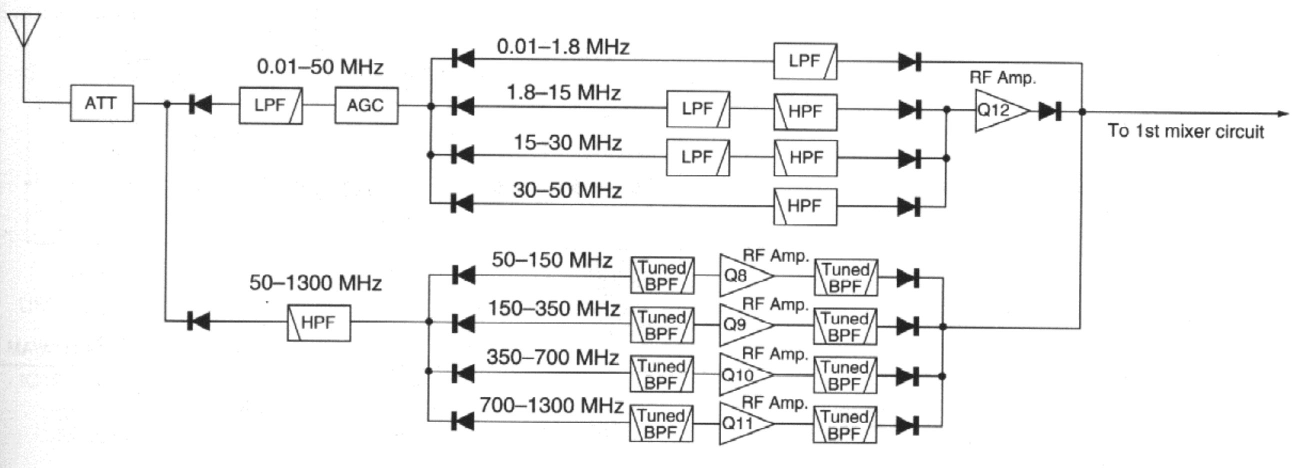
The VHF/UHF RF circuit amplifies the received signals within the range 50–1300 MHz and filters out-of-band signals.

The VHF/UHF RF circuit consists of 4 bands of filter circuits with an RF amplifier for each.

The 50–149.999999 MHz signals from the RF filter pass through high-pass filter (D11, L17, C53–C55, D12, D82, D83, L18, C57) via the band switching diode (D10), and are then amplified at the RF amplifier (Q8) between the tunable bandpass filters (D13, D80, L19–L21, D14, D81, L23–L25). The filtered signals are applied to the 1st mixer circuit (IC4) via the band switching diode (D15).

For improving the characteristic of the bandpass filter circuit, the shift switch (Q84) shifts the cut off frequency of the high-pass filter (D12, D82, D83, L18, C57). The shift switch (Q84) is controlled by the VCO 1 signal from the DDS IC (IC18).

• RF filter and amplifier circuits



The 150–349.999999 MHz signals from the band switching diode (D16) pass through the high-pass filter (L27–L29, C69–C74) and tunable bandpass filter (D18, L31–L33), and are then amplified at the RF amplifier (Q9) and pass through another tunable bandpass filter (D19, L35–L37). The filtered signals are applied to the 1st mixer circuit (IC4) via the band switching diode (D20).

The 350–699.999999 MHz signals from the band switching diode (D21) pass through the high-pass filter (L40, C92–C94, C619) and tunable bandpass filter (D23, D76, L41, L42). The filtered signals are then amplified at the RF amplifier (Q10) and pass through the tunable bandpass filters (D24, D77, L45–L47). The filtered signals are applied to the 1st mixer circuit (IC4) via the band switching diode (D25).

The 700–1300 MHz signals from the band switching diode (D26) pass through the high-pass filter (L141, C110, C606) and 2-stage tunable bandpass filters (D78, D79, L163, D29, D30, L51–L53). The filtered signals are then amplified at the RF amplifier (Q11) and pass through the tunable bandpass filters (D31, D32, L55, L56). The filtered signals are applied to the 1st mixer circuit (IC4) via the band switching diode (D33).

The tunable bandpass filters employ varactor diodes to tune the center frequency of the RF passband for wide bandwidth receiving and good image response rejection. These diodes are controlled by TUNV signal from the CPU (LOGIC unit; IC1, pin 37) via the tune controller (LOGIC unit; IC11b).

• Tunable bandpass filters

Receive freq. (MHz)	BPF select signal	Varactor diodes	RF amp.
50.0–149.999999	B0	D11–D14, D80–D83	Q8
150.0–349.999999	B1	D18, D19	Q9
350.0–699.999999	B2	D23, D24, D76, D77	Q10
700.0–1300.0	B3	D29–D32, D78, D79	Q11

4-1-5 1ST MIXER CIRCUIT (RF UNIT)

The 1st mixer circuit converts the received RF signals to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will pass through the bandpass filters at the next stage of the 1st mixer.

The filtered RF signals are mixed with 1st LO signals at the 1st mixer circuit (IC4) to produce a 266.7 MHz 1st IF signal. The 1st IF signal is output from pin 5, and passed through the bandpass filter (FI1) to suppress unwanted harmonic components. The filtered 1st IF signal is applied to the IF circuit.

The 1st LO signals are generated at the VCO-1 (Q14, Q15) or VCO-2 (Q18, Q19) circuit (according to the receiving frequency band) and are amplified at the buffer amplifier (IC26). The amplified signals are then applied to the 1st mixer (IC4, pin 2) directly or passed through the divider circuit (IC6).

4-1-6 1ST IF AND 2ND MIXER CIRCUITS (RF UNIT)

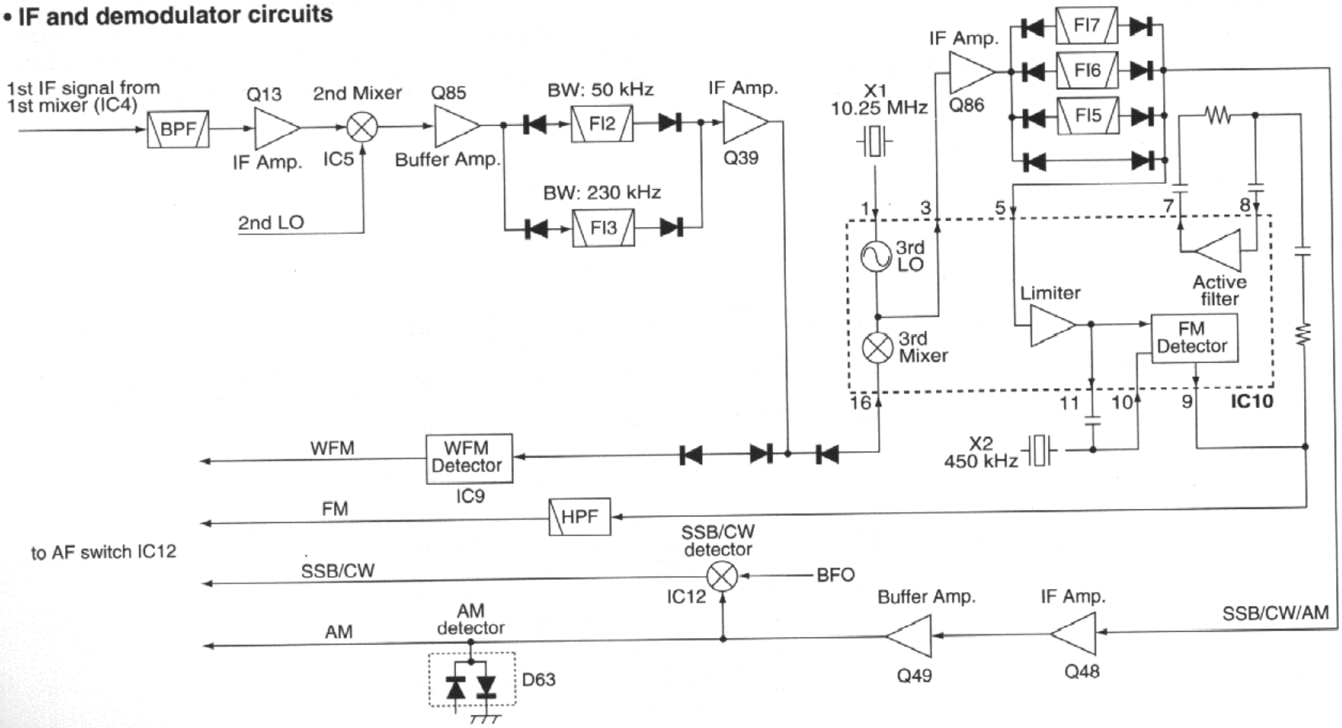
The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal.

The filtered 266.7 MHz 1st IF signal from the bandpass filter (FI1) is amplified at the 1st IF amplifier (Q13) then mixed with the 2nd LO signal at the 2nd mixer circuit (IC5) to produce a 10.7 MHz 2nd IF signal. The 2nd IF signal is passed through one of 2 bandpass filters (FI2 or FI3; depending on the selected mode and bandwidth) after being amplified at the IF amplifier (Q85). The filtered 2nd IF signal is amplified at the buffer amplifier (Q39), then applied to the WFM demodulator or 3rd IF circuit.

4-1-7 3RD MIXER CIRCUIT (RF UNIT)

The 3rd mixer circuit mixes the 2nd IF signal and 3rd LO signal to produce a 450 kHz 3rd IF signal (except WFM mode).

• IF and demodulator circuits



The 10.7 MHz 2nd IF signal from the buffer amplifier (Q39) is applied to the 3rd mixer section in the FM IF IC (IC10, pin 16). The applied signal is mixed with a 3rd LO signal generated by X1 (10.25 MHz) to produce a 450 kHz 3rd IF signal.

The 3rd IF signal is output from pin 3, and passed through one of 3 bandpass filters (FI5, FI6 or FI7) or bypassed, according to the selected mode and bandwidth after being amplified at the IF amplifier (Q86). The filtered or bypassed signal is applied to the each demodulator circuit (except WFM mode).

• Bandpass filter selection

Modes	Bandpass filter	Passband width
AM, SSB, CW	FI5	2.8 kHz
FM, AM, SSB, CW	FI6	6 kHz
FM, AM	FI7	15 kHz

4-1-8 DEMODULATOR CIRCUITS (RF UNIT)

The demodulator circuit converts the 2nd IF signal into AF signals. 4 separate demodulator circuits are employed for each mode.

(1) WFM mode

The 10.7 MHz 2nd IF signal from the buffer amplifier (Q39) is applied to the WFM demodulator circuit (IC9, pin 2).

The applied IF signal is amplified at the IF amplifier section in the IC9 and then output from pin 10. The output signal is applied to the quadrature detector section (pin 11) to demodulate AF signals. The demodulated AF signals are applied to the AF switch circuit via the de-emphasis circuit (R179, C285).

(2) FM mode

The filtered or bypassed 3rd IF signal is applied to the quadrature detector section in the FM IF IC (IC10, pin 10) then mixed with the signal generated by the discriminator (X2) to demodulate AF signals. The AF signals are output from pin 9 and applied to the AF switch circuit via the high-pass filter circuit (IC11).

(3) AM mode

The filtered 3rd IF signal from the one of 3 bandpass filters (FI5, FI6 or FI7) is amplified at the IF and buffer amplifiers (Q48, Q49). The amplified IF signal is applied to the AM detector circuit (D63) to be converted into AF signals, and the AF signals are applied to the AF switch circuit.

(4) SSB and CW modes

The amplified 3rd IF signal from the buffer amplifier (Q49) is applied to the mixer circuit (IC12, pin 6) and mixed with the BFO signal generated by the BFO circuit for demodulation. The demodulated AF signals are applied to the AF switch circuit.

4-1-9 AF SWITCH CIRCUIT (RF UNIT)

The demodulated AF signals from the demodulator circuits are applied to the AF switch (IC14). This consists of 4 analog switches which are selected with a mode signal from the CPU (LOGIC unit; IC1) via the I/O expander (IC3). The switched AF signals are applied to the AF circuit.

4-1-10 AF CIRCUIT (RF AND LOGIC UNITS)

The switched AF signals from the AF switch circuit are amplified at the AF amplifier circuit (RF unit; Q56) and then applied to the LOGIC unit.

The AF signals from the RF unit are applied to the electronic volume control circuit (LOGIC unit; IC9a, pin 1). The level controlled AF signals are output from pin 2 and applied to the AF power amplifier (LOGIC unit; IC10, pin 4). The power amplified AF signals are passed through the AF level control switch (LOGIC unit; S1) then applied to the internal speaker via the [EXT SP] jack.

The electronic volume control circuit controls AF gain, therefore, the AF output level varies according to the [VOL] setting and also the squelch conditions.

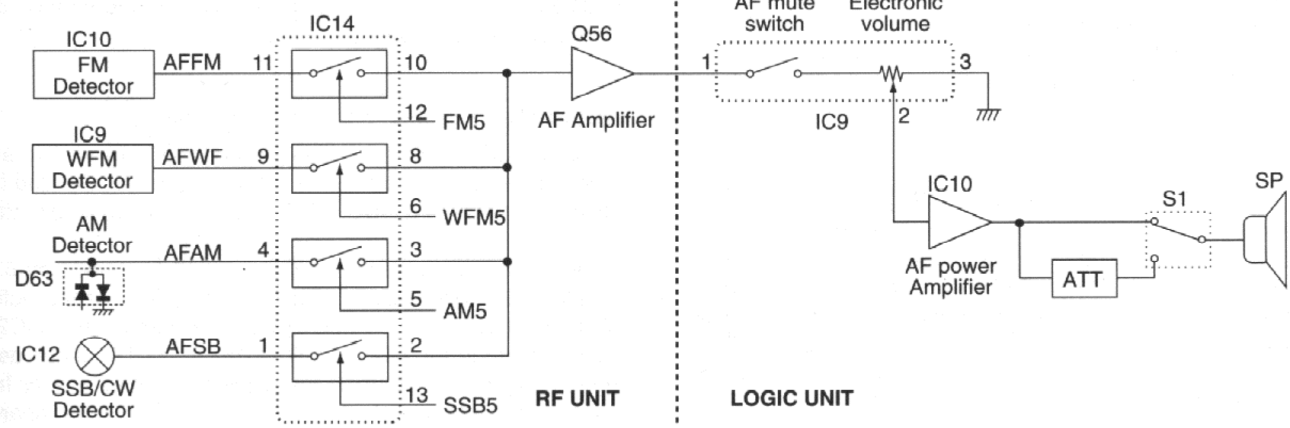
4-1-11 SQUELCH CIRCUIT (RF AND LOGIC UNITS)

A squelch circuit cuts out AF signals when no RF signal is received or when the S-meter signal is lower than the [SQUELCH] control setting level. By detecting noise components in the AF signals, the CPU controls the electronic volume control circuit.

• NOISE SQUELCH

Some noise components in the AF signals from pin 9 of the FM IF IC (IC10) are applied to the noise amplifier section in the IC (IC10, pin 8). The amplified signals are output from pin 7, and applied to the electronic volume control circuit (LOGIC unit; IC9b, pin 8) and level controlled noise components are output from pin 7. The output signals are applied to the noise amplifiers (LOGIC unit; Q6, Q7) to be converted into pulse-type signals, then applied to the CPU (LOGIC unit; IC1, pin 39) as an NOIN signal.

• Squelch and AF amplifier circuits



• S-METER SQUELCH

The S-meter signal is applied to the CPU from the meter amplifier circuit (RF unit; IC13a) via the SMAD line, and also the S-meter squelch setting level is applied to the CPU. The CPU compares these signals, then outputs a control signal to the electronic volume control circuit (RF unit; IC9a) to cut out AF signals.

4-1-12 NOISE BLANKER CIRCUIT (RF UNIT)

The noise blanker circuit detects pulse-type noise, and stops IF amplifier operation during detection. The noise blanker function activates only when SSB, CW or AM mode is selected.

A portion of the filtered 2nd IF signal from one of 2 bandpass filters (FI2 or FI3) is amplified at the NB amplifier (Q41) then applied to the WFM IF IC (IC9, pin 2). The applied signal is amplified at the IF amplifier section in the IC, then output from pin 10. The output signal is rectified at the NB detector circuit (D53) to be converted into DC voltage after being amplified at the noise amplifier (Q35). The DC voltage is applied to the NB gate control circuit (Q37, Q38) to control the NB gate (Q40).

Some DC voltage is fed back to the IF amplifier section in the WFM IF IC (IC9, pin 3). The IF amplifier functions as an AGC circuit to reduce average noise. Therefore, the noise blanker function shuts off pulse-type noise only.

4-1-13 AGC CIRCUIT (RF UNIT)

The AGC (Auto Gain Control) circuit reduces IF amplifier gain to keep the audio output at a constant level.

An RSSI signal is used for AGC function from the WFM IF IC (IC9, pin 17) while in WFM mode, or used from the FM IF IC (IC10, pin 12) while in FM, AM, SSB or CW (except WFM) mode.

The RSSI output signal is applied to the IF amplifiers (Q13, Q39) after being amplified at the AGC amplifier (Q33) during WFM operation. In other modes, the RSSI signal is amplified at the AGC amplifier (Q51), passes through the time constant circuit (Q52, Q53, R284, R290, R291, C371–C373) and is then applied to the IF amplifiers (Q13, Q39). The AGC control signal is applied to the VHF/UHF tunable bandpass filters after being amplified at the VHF/UHF AGC amplifier (IC13b).

AGC speed is controlled by changing the time constant at the AGC control line with resistors (R284, R290, R291) and capacitors (C371–C373). R290 and C372 are used for AGC slow, and R284 and C371 are used for AGC fast mode's time constant. However, R291 and C373 are connected to the AGC control line while scanning to obtain the fastest AGC response.

4-1-14 VSC CIRCUIT (LOGIC UNIT)

The VSC (Voice Scan Control) detects AF signals and mutes undesired signals such as unmodulated, beat and noise component signals. When the VSC function is ON and an unmodulated signal is received, squelch functions the same as closed (no signal condition) even when it's open, or the scan function resumes for a short period on any scan setting during scanning.

A portion of the AF signals from the AF amplifier (RF unit; Q56) is applied to the VSC control circuit (IC15, pin 16) to detect demodulated signals while the VSC function is ON. When audio (voice) component signals are included in the AF signals, the VSC IC (IC15) outputs a low level signal from pin 13 to the CPU (IC1, pin 45) to release the mute switch (IC9).

4-1-15 S-METER CIRCUIT (RF UNIT)

The S-meter circuit indicates the relative received signal strength while receiving and changes depending on the received signal strength.

A portion of the AGC signal is applied to the meter amplifier circuit (IC13a). The amplified signal is then applied to the CPU (LOGIC unit; IC1, pins 31) as an SMAD signal to drive the S-meter.

The SMAD signal is also used for noise and S-meter squelch operation by comparison with the [SQUELCH] control setting level and received signal strength at the CPU.

4-2 PLL CIRCUITS

4-2-1 1ST LO PLL CIRCUIT (RF UNIT)

The 1st LO circuit generates the 1st LO frequencies, and the signals are applied to the 1st mixer circuit. The 1st LO circuit consists of a VCO-1/2 circuit and PLL IC, etc.

The generated signal from VCO-1 (Q14, Q15) or VCO-2 (Q18, Q19) is applied to the prescaler section in the PLL IC (IC7, pin 11) after being amplified at the buffer amplifiers (IC26, Q27). The applied signal is prescaled in the PLL IC based on the divided ratio (N-data) to produce approx. 50 kHz signals which are applied to the phase detector section.

The generated reference signal from the reference oscillator (X1; 10.25 MHz) is amplified at the buffer amplifiers (Q22, Q42) and is applied to the programmable divider section in the PLL IC (IC7, pin 20). The applied signal is prescaled in the PLL IC based on the divided ratio (1/205) to produce approx. 50 kHz phase signals. The reference phase signals are applied to the phase detector section.

The phase detector section compares 2 of the applied phase signals. The phase detected signals are passed through the charge pump section and then output from pin 6 of the PLL IC. The output signals are applied to the loop filter circuit (Q25, Q26) to be converted into DC voltage as a PLL lock voltage. The lock voltage is applied to the CPU (LOGIC unit; IC1, pin 33) as an L1AD signal to control the VHF/UHF tunable bandpass filter.

4-2-2 2ND LO PLL CIRCUIT (RF UNIT)

The 2nd LO circuit generates the 2nd LO frequencies, and the signals are applied to the 2nd mixer circuit. The 2nd LO circuit consists of a DDS, VCO-3 and loop filter circuit, etc.

The generated signal from VCO-3 (Q76) is divided by 8 at the divider circuit (IC23) after being amplified at the buffer amplifier (Q77). The divided signal is then amplified at IC28, and applied to the DDS circuit (IC18). The DDS circuit generates digital signals using the applied signal as a clock frequency. The phase detector section in the DDS IC compares it's phase with the divided reference frequency (3.41 MHz) which is generated at the reference oscillator (X1).

The D/A converter (R351–R374), bandpass filter (L117, L118, L175, C496–C503) and buffer amplifier (IC19) circuits are connected to the DDS output to convert the digital oscillated signals into smooth analog signals.

4-2-3 BFO CIRCUIT (RF UNIT)

The BFO signals are generated by the DDS circuit (IC25) using the divided reference signal. 10-bit digital signals are converted into 447.3–452.7 kHz analog wave signals at the D/A converter (R423–R442). The converted analog wave signals are passed through the bandpass filter (L99–L101, C269–C274) via the switching diode (D52), then applied to the mixer circuit (IC12).

4-3 SCOPE CIRCUIT

4-3-1 SCOPE RECEIVER CIRCUIT (RF UNIT)

A portion of the 10.7 MHz 2nd IF signal from the 2nd mixer circuit (IC5) passes through the bandpass filter (FI8) to suppress out-of-band signals, and is then mixed with a scope LO signal at the mixer section in the FM IF IC (IC8, pin 15), which includes the RSSI terminal, to produce a 450 kHz scope IF signal. The mixed IF signal is filtered at the ceramic bandpass filter (FI4) then applied to the limiter amplifier section in the FM IF IC (IC8, pin 5). The applied IF signal is converted into DC voltages according to the applied IF signal strength at the RSSI section in the IC.

The converted voltages are applied to the CPU (LOGIC unit; IC1, pin 34) as an SCAD signal.

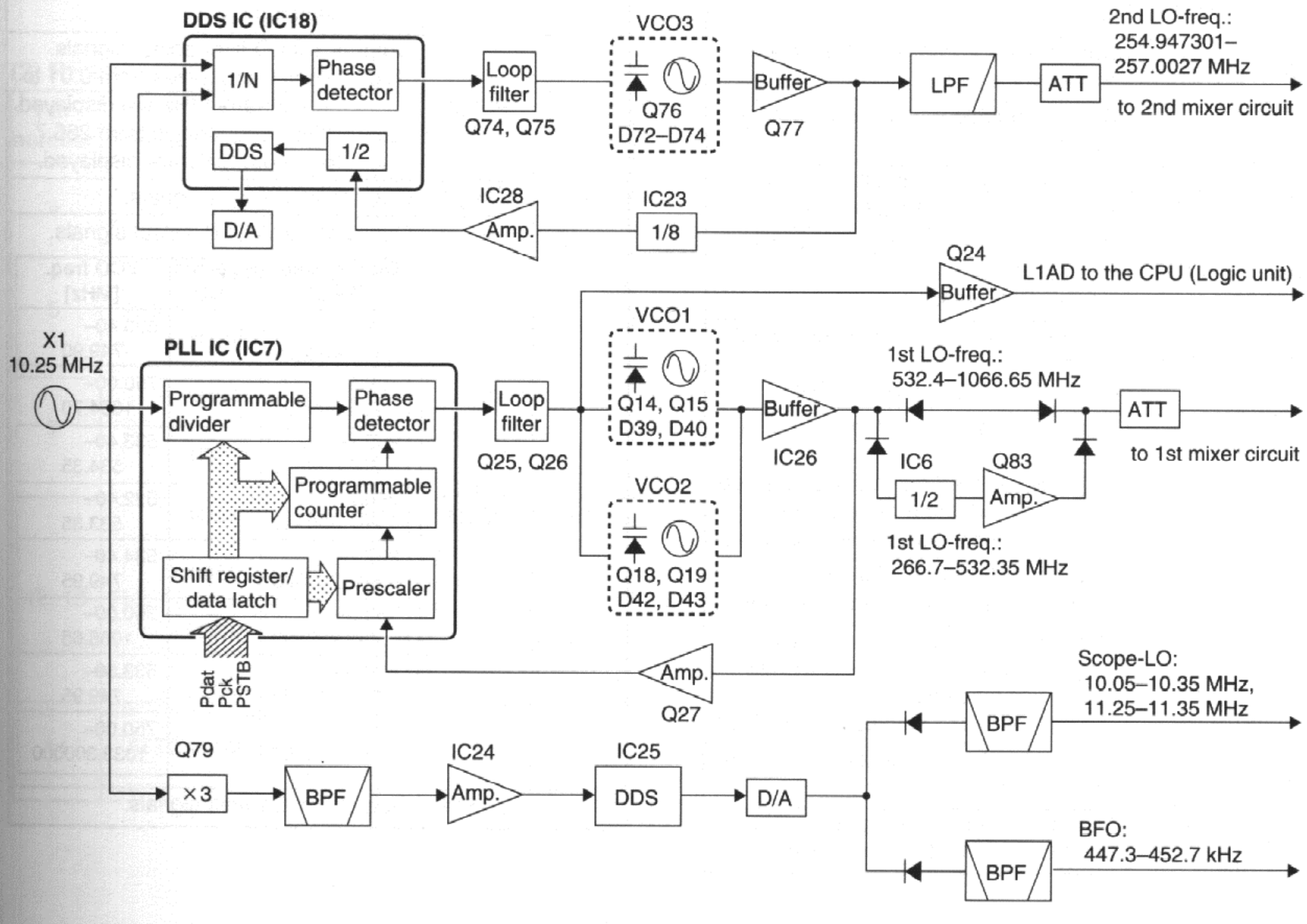
The sweeping scope LO signals generated by IC25 (10.05–10.35 MHz/11.25–11.35 MHz) are applied to the mixer section in the FM IF IC, when the scope function is activated.

4-4 POWER SUPPLY CIRCUITS

4-4-1 VOLTAGE LINES (LOGIC UNIT)

Line	Description
ACHV	The voltage from a DC power supply.
HV	The same voltage as the ACHV line which is controlled by the [POWER] switch.
RF+5	Common 5 V line converted from the HV line by the RF+5 regulator circuit (IC5).
RF+8	Common 8 V line converted from the HV line by the RF+8 regulator circuit (IC6).
RF33	Common 33 V line converted from the HV line by the 33 V DC-DC convertor circuit (IC7). The output voltage is applied to the PLL circuit (RF unit).
RF–5	Common –5 V line converted from the RF+8 line by the –5 V DC-DC convertor circuit (IC8).
L+5	Common 5 V line converted from the HV line by the L+5 regulator circuit (IC4).

• PLL circuits



4-5 PORT ALLOCATIONS

4-5-1 CPU (LOGIC unit; IC1)

Pin number	Port name	Description
1	RES	Input port for the reset signal.
2, 3	ETAL, EXTAL	Input ports for the CPU system clock oscillator (X1; 9.8304 MHz).
10	RXD	Input port for data signal from the connected PC via the RS-232C interface IC (IC3).
11	TXD	Outputs data signal to the connected PC via the RS-232C interface IC (IC3).
17	ECK	Outputs clock signal to the EEPROM IC (IC13).
18	EDAT	Outputs data signal to the EEPROM IC (IC13).
21	DSTD	Input port for the DTMF latch data.
22–25	DQ4– DQ1	Input ports for the DTMF decode signals.
27	Mck	Outputs serial clock signal for the electronic volume IC (IC9) and output expander ICs (RF unit; IC1– IC3).
28	Mdat	Outputs serial data signal for the electronic volume IC (IC9) and output expander ICs (RF unit; IC1– IC3).
31	SMAD	Input port for S-meter signal.
32	CMAD	Input port for center indicator signal.
33	L1AD	Input port for 1st LO PLL lock voltage.
34	SCAD	Input port for the scope signal.
35	CTAD	Input port for the CTCSS decoded signal.
36	REDA	Output port for reference frequency control voltage.
37	TUDA	Outputs tunable bandpass filter control voltage.
39	NOIN	Input port signal strength detection signal (NOIN; pulse-type).
40	LCT	Input port for unlock signal from the PLL IC (RF unit; IC7). High : PLL unlock
41	POCO	Outputs power switching circuit control signal. High: While turning power ON.
43	VSSW	Output VSC-time constant control signal. High: Modulated signals are received. Low : Unmodulated or beat signals are received or while scanning.
44	VSON	Outputs VSC control signals. Low : When the VSC function is ON.
45	VSC	Input port for VSC detected signals. High: Unmodulated or beat signals are received. Low : Modulated signals are received.
46	AFST	Outputs strobe signals for the volume control IC (IC9).
48–50	CON2– CON0	Output mode control signals for the 2nd LO DDS IC (RF unit; IC18).

CPU (IC1) — continued

Pin number	Port name	Description
51	STD2	Outputs strobe signals for the BFO/scope DDS IC (RF unit; IC25).
52	STD1	Outputs strobe signals for the 2nd LO DDS IC (RF unit; IC18).
53	PSTB	Outputs strobe signals for the PLL IC (RF unit; IC7).
54	Pdat	Outputs serial data signals for the PLL IC (RF unit; IC7) and DDS ICs (RF unit; IC18, IC25).
55	Pck	Outputs serial clock signal for the PLL IC (RF unit; IC7) and DDS ICs (RF unit; IC18, IC25).
58–60	MST3– MST1	Outputs strobe signals for the output expander ICs (RF unit; IC1–IC3).
61	DRES	Outputs reset signal for the DDS ICs (RF unit; IC18, IC25).

4-5-2 DDS (RF unit; IC18)

<table>
<tr><th>Pin number</th><th>Port name</th><th>Description</th></tr>
<tr><td>68</td><td>PFIL4</td><td>Outputs scope LO select signals.
High: When Scope function is ON.</td></tr>
<tr><td>69</td><td>PFIL3</td><td>Outputs BFO select signals.
High: When SSB or CW mode is selected.</td></tr>
<tr><td>70</td><td>PFIL2</td><td>Outputs 1st LO filter select signals.
High: When frequencies from 0.01 to 265.699999 MHz are displayed.
Low : When frequencies from 265.7 to 1300.0 MHz are displayed.</td></tr>
<tr><td>72</td><td>VSFT2</td><td>Outputs VCO2 shift signals.</td></tr>
<tr><td>73,
75</td><td>VCO2,
VCO1</td><td>Output VCO2/VCO1 select signals.
<table>
<tr><th>Display freq. [MHz]</th><th>Selected VCO</th><th>VCO freq. [MHz]</th></tr>
<tr><td>0.01–108.299999</td><td>VCO1</td><td>533.40–749.90</td></tr>
<tr><td>108.3–265.699999</td><td>VCO2</td><td>750.00–1064.70</td></tr>
<tr><td>265.7–266.699999</td><td>VCO1</td><td>533.40–534.35</td></tr>
<tr><td>266.7–267.699999</td><td>VCO1</td><td>532.40–533.35</td></tr>
<tr><td>267.7–483.299999</td><td>VCO1</td><td>534.40–749.95</td></tr>
<tr><td>483.3–799.999999</td><td>VCO2</td><td>750.00–1066.65</td></tr>
<tr><td>800.0–1016.699999</td><td>VCO1</td><td>533.30–749.95</td></tr>
<tr><td>1016.7–1300.000000</td><td>VCO2</td><td>750.00–1033.300000</td></tr>
</table></td></tr>
<tr><td>74</td><td>VSFT1</td><td>Outputs VCO1 shift signals.</td></tr>
</table>

4-5-3 OUTPUT EXPANDER IC

(1) RF unit; IC1

Pin number	Port name	Description
4	B0C	Outputs low-pass filter select signal. High: When frequencies below 1.8 MHz are displayed.
5	B1C	Outputs bandpass filter select signal. High: When frequencies from 1.8 to 14.999999 MHz are displayed.
6	B2C	Outputs bandpass filter select signal. High: When frequencies from 15.0 to 29.999999 MHz are displayed.
7	B3C	Outputs bandpass filter select signal. High: When frequencies from 30.0 to 49.999999 MHz are displayed.
11	B7C	Outputs bandpass filter select signal. High: When frequencies from 700.0 to 1300.0 MHz are displayed.
12	B6C	Outputs bandpass filter select signal. High: When frequencies from 350.0 to 699.999999 MHz are displayed.
13	B5C	Outputs bandpass filter select signal. High: When frequencies from 150.0 to 349.999999 MHz are displayed.
14	B4C	Outputs bandpass filter select signal. High: When frequencies from 50.0 to 149.999999 MHz are displayed.

(2) RF unit; IC2

<table>
<tr><th>Pin number</th><th>Port name</th><th>Description</th></tr>
<tr><td>4</td><td>NB</td><td>Outputs NB control signals.
High: While NB fuction is ON. (SSB/CW mode only)</td></tr>
<tr><td>5</td><td>AGCF</td><td>Outputs AGC time constant control signals.
High: When WFM or FM mode is selected (AGC-fast).</td></tr>
<tr><td>7</td><td>SCAN</td><td>Outputs AGC time constant control signals.
High: While scanning (fastest AGC speed).</td></tr>
<tr><td>12, 13</td><td>FL5, FL4</td><td>Output 10.7 MHz IF filter select signals.
<table>
<tr><th>SW signal</th><th>Bandpass filter</th><th>Passband width</th></tr>
<tr><td>FL4</td><td>FI2</td><td>50 kHz</td></tr>
<tr><td>FL5</td><td>FI3</td><td>230 kHz</td></tr>
</table></td></tr>
<tr><td>14</td><td>ATTC</td><td>Outputs attenuator control signals.
High: When attenuator function is ON.</td></tr>
</table>

(3) RF unit; IC3

<table>
<tr><th>Pin number</th><th>Port name</th><th>Description</th></tr>
<tr><td>4</td><td>WFM</td><td>Outputs WFM mode select signals.
High: When WFM mode is selected.</td></tr>
<tr><td>5</td><td>FM</td><td>Outputs FM mode select signals.
High: When FM mode is selected.</td></tr>
<tr><td>6</td><td>AM</td><td>Outputs AM mode select signals.
High: When AM mode is selected.</td></tr>
<tr><td>7</td><td>SSB</td><td>Outputs SSB mode select signals.
High: When SSB mode is selected.</td></tr>
<tr><td>11–14</td><td>FL3–FL0</td><td>Output 450 kHz IF filter select signals.
<table>
<tr><th>SW signal</th><th>Bandpass filter</th><th>Passband width</th></tr>
<tr><td>FL0</td><td>FI5</td><td>2.8 kHz</td></tr>
<tr><td>FL1</td><td>FI6</td><td>6 kHz</td></tr>
<tr><td>FL2</td><td>FI7</td><td>15 kHz</td></tr>
<tr><td>FL3</td><td>By-pass</td><td>—</td></tr>
</table></td></tr>
</table>

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION BEFORE SERVICING

The receiver (IC-PCR1000) can be adjusted by sending adjustment data to the RS-232C port via a PC. Most of the adjustments in this section must use **EX-2099,** an adjustment program for IC-PCR1000. The software that comes with the IC-PCR1000 is not necessary for adjustments in this section.

■ SYSTEM REQUIREMENTS

- IBM PC compatible computer
- An RS-232C serial port (38400 bps or faster)
- Microsoft Windows 95
- Intel i486DX4 processor or faster (pentium 100 MHz or faster recommended)
- At least 16 MB RAM
- At least 10 MB of hard disk space
- 640 × 480 pixel display (800 × 600 pixel display recommended)

■ SOFTWARE INSTALLATION

NOTE: Before using the program, make a backup copy of the original disk. After making a backup copy, keep the original disk in a safe place.

① Boot up Windows.
  - Quit all applications when Windows is running.

② Insert the backup disk 1 into the appropriate floppy drive.

③ Select 'Run' from the [Start] menu.

④ Type the setup program name using the full path name, then push the [Enter] key. (A:\ setup [Enter])

⑤ Follow the prompts.

⑥ Program group 'IC-PCR1000' appears in the 'Programs' folder of the [Start] menu.

■ OPERATING INSTRUCTIONS

The adjustment program window contains 3 panels; the Power Panel, Control Panel and Adjustment Panel. The Power Panel will appear at start up the program.

① Connect IC-PCR1000 and PC with an RS-232C serial cable.

② Boot up Windows.

③ Click the "EX-2099 for IC-PCR1000" in the program group 'IC-PCR1000' to start the program.
  - The Power Panel appears.

④ Click "POWER ON" on the Power panel.
  - Control Panel and Adjustment Panel appear.

⑤ Click "START" on the Adjustment Panel when starting the SOFTWARE adjustment.
  - Data panel appears at the bottom side of the Adjustment panel.

⑥ Click "Read ALL DATA" on the Adjustment Panel.
  - Application reads adjustment data of the connected receiver.

⑦ Set or modify adjustment data as desired. See the following SOFTWARE adjustments.

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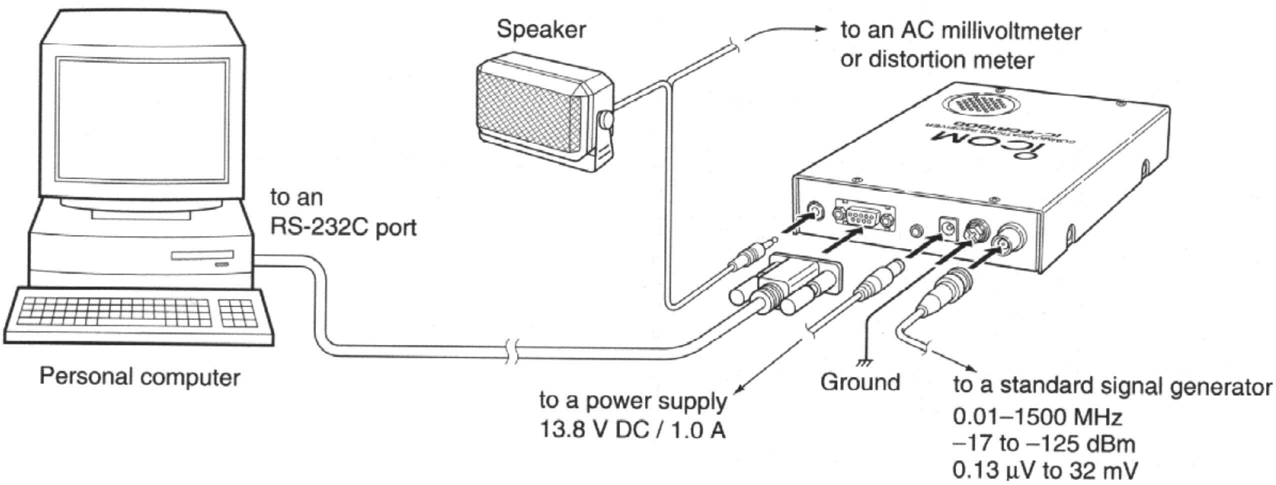
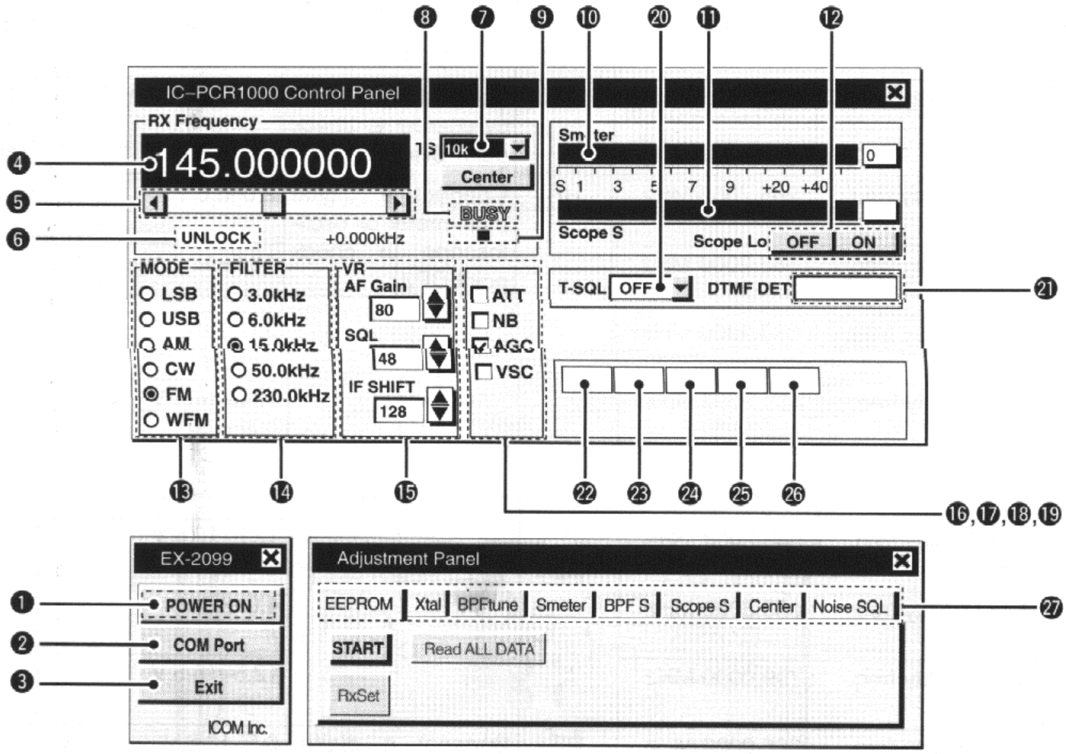
■ BASIC CONNECTION



■ PANEL DESCRIPTIONS



♦ POWER PANEL

1 POWER button
Turns IC-PCR1000 on and off.

2 COM port button
Used to select a COM port.

3 EXIT button
Quits the program.

♦ CONTROL PANEL

4 FREQENCY indication
Indicates or inputs the receive frequency.

5 FREQUENCY scroll bar
Used to change the receive frequency. Moving the button to the right increases the frequency; to the left decreases the frequency.

6 UNLOCK indicator
Appears when the PLL is unlocked.

7 Tuning step button
Used to change the tuning step.

8 BUSY indicator
Appears when receiving a signal or when signal noise opens the squelch.

9 FM center indicator
Indicates the tuning level when selecting the 6 kHz or 15 kHz IF filter in FM mode.

10 S-meter indicator
Indicates the receive signal strength.

11 Scope S indicator

12 Scope Lo (ON/OFF) button

13 Receive mode buttons
Select a receive mode.

14 FILTER (IF filter) buttons
Change the IF filter in use.

15 Volume buttons
Adjust the audio output, squelch level and set the signals passband position.

16 ATT (Attenuator) button
Turns the attenuator on and off.

17 NB (Noise Blanker) button
Turns the noise blanker function on and off. The noise blanker is used to reduce pulse type noise.

18 AGC (Automatic Gain Control) button
Turns the AGC function on and off.

19 VSC (Voice Scan Control) button
Turns the voice scan control function on and off. This function detects whether signals are modulated (contain voice or music components, etc.) or not.

20 T-SQL (Tone squelch) button
Indicates or selects tone frequency for the tone squelch.

21 DTMF decode indicator
Indicates the decoded DTMF signals.

22 AD1 (SMAD) indicator
Indicates voltage level for the S-meter.

23 AD2 (CMAD) indicator
Indicates voltage level for the center meter.

24 AD3 (L1AD) indicator
Indicates the 1st LO PLL lock voltage level.

25 AD4 (SCAD) indicator
Indicates voltage level for the scope signal.

26 AD5 (CTAD) indicator
Indicates voltage level for the CTCSS decoded signal.

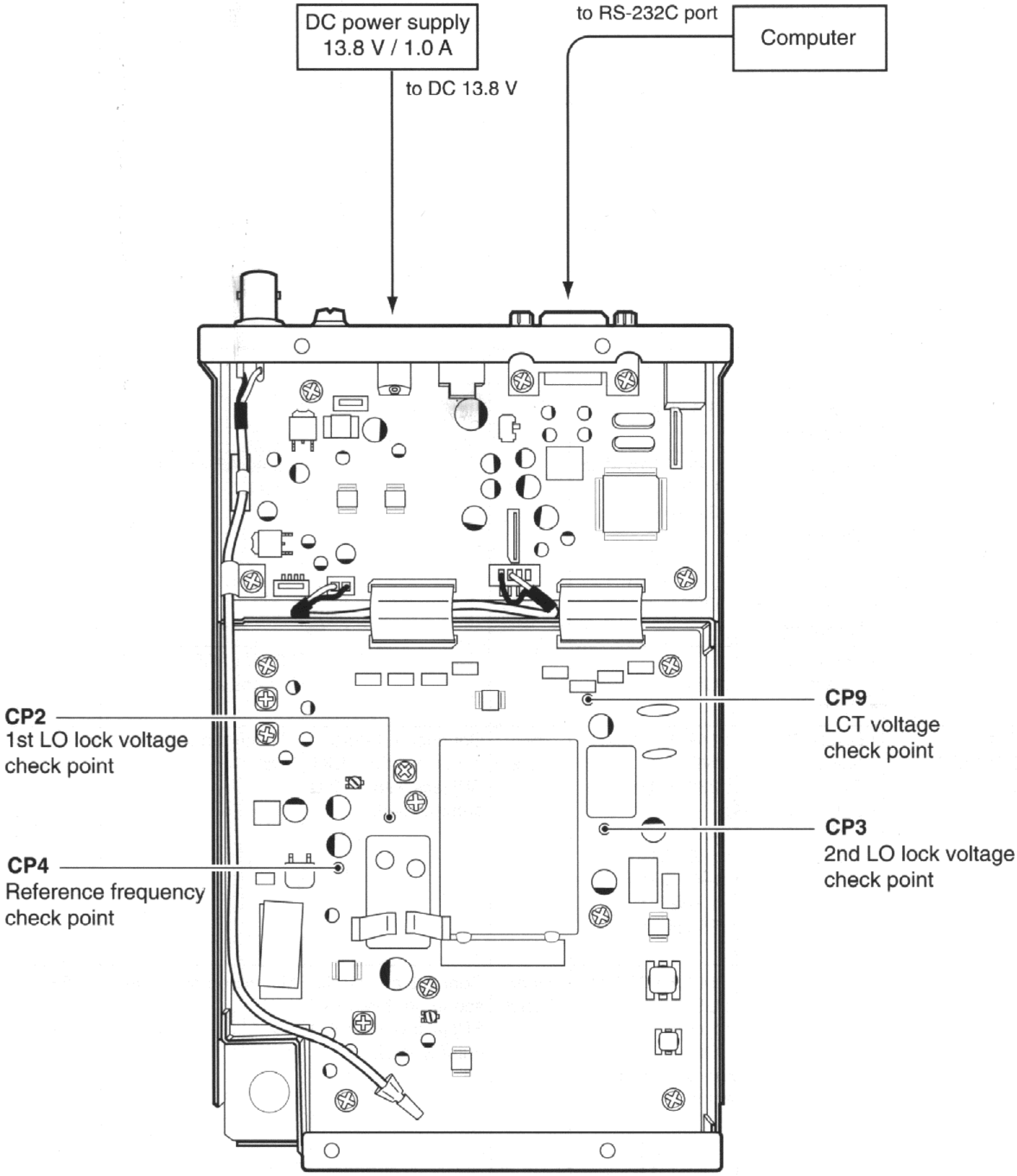
♦ ADJUSTMENT PANEL

27 Item select buttons
Used to select the adjustment items.

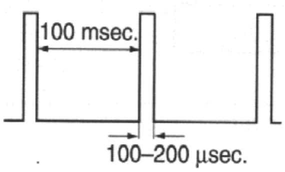
5-2 PLL ADJUSTMENT AND IF PEAK ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT
			UNIT	LOCATION		
REFERENCE FREQUENCY	1	• Display freq. : Any	RF	Connect a frequency counter to check point CP4.	10.250000 MHz	Use the adjustment software. **(see page 5-6)**
1ST LO PLL LOCK VOLTAGE	1	• Display freq. : 265.7000 MHz	RF	Connect a digital multi-meter or oscilloscope to check point CP2.	2.0–6.0 V	Verify
	2	• Display freq. : 383.2000 MHz			13.5–17.7 V	
	3	• Display freq. : 383.3000 MHz			3.0–7.0 V	
	4	• Display freq. : 483.2000 MHz			10.0–14.0 V	
	5	• Display freq. : 483.3000 MHz			1.5–5.5 V	
	6	• Display freq. : 633.2000 MHz			12.5–16.5 V	
	7	• Display freq. : 633.3000 MHz			4.0–8.0 V	
	8	• Display freq. : 799.9000 MHz			12.5–16.5 V	
2ND LO PLL LOCK VOLTAGE	1	• Display freq. : 265.0000 MHz	RF	Connect a digital multi-meter or oscilloscope to check point CP3.	6.5–10.5 V	Verify
	2	• Display freq. : 266.0000 MHz			6.6–10.6 V	
	3	• Display freq. : 267.0000 MHz			6.4–10.4 V	
LCT TERMINAL	1	• Display freq. : Any frequency of the 1st LO and 2nd LO are locked.	RF	Connect a digital multi-meter or oscilloscope to check point CP9.	Less than 1.5 V	Verify
IF PEAK	1	• Display freq. : 130.0200 MHz • Mode : FM • AGC : ON • Filter : 15 kHz • R521 (RF unit) : Center • R523 (RF unit) : Center • Connect a standard signal generator to [ANT] and set as: Frequency : 130.0200 MHz Level : 50 μV* (–73 dBm) Modulation : OFF • Receiving			Maximum S-meter level	Use the adjustment software. **(see page 5-6, Tuned BPF)**
	2	• Display freq. : 149.9800 MHz • Set an SSG as : Frequency : 149.9800 MHz • Receiving				

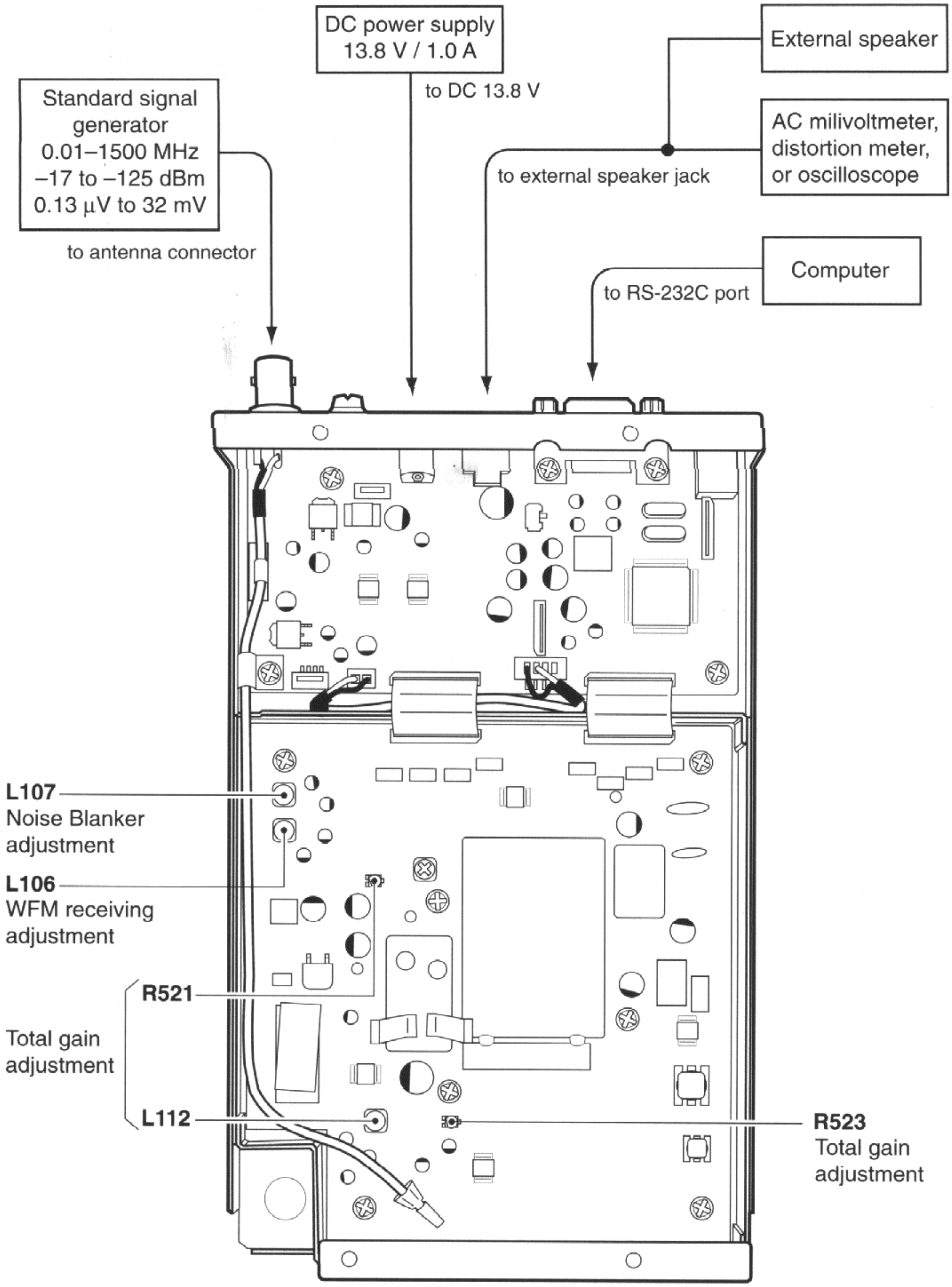
*This output level of a standard signal generator (SSG) is indicated as SSG's open circuit.


DC power supply
13.8 V / 1.0 A
to DC 13.8 V
to RS-232C port
Computer
CP2
1st LO lock voltage
check point
CP4
Reference frequency
check point
CP9
LCT voltage
check point
CP3
2nd LO lock voltage
check point

5-3 RECEIVE ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
			UNIT	LOCATION		UNIT	ADJUST
TOTAL GAIN	1	• Display freq. : 149.97000 MHz • Mode : USB • Filter : 3.0 kHz • Set an SSG as : Frequency : 149.97015 MHz Level : 1.8 µV* (–102 dBm) Modulation : OFF • Receiving	Rear Panel	Connect an AC millivoltmeter to the [EXT SP] jack with an 8 Ω dummy load.	Maximum AF level	RF	L112
	2	• Display freq. : 149.97000 MHz • Mode : FM • Filter : 15.0 kHz • Set an SSG as : Mode : FM Level : 1.0 mV* (–47 dBm) Modulation : 1 kHz Deviation : 3.5 kHz • Receiving			Any AF level	Computer display	AF Gain
	3	• Display freq. : 149.97015 MHz • Mode : USB • Filter : 3.0 kHz • Set an SSG as : Level : 1.0 mV* (–47 dBm) Modulation : OFF • Receiving			Same AF level as step 2	RF	R523
	4	• Set an SSG as : Level : OFF • Receiving			20 dB of AF level difference as step 3		R521
WFM RECEIVER	1	• Display freq. : 149.97000 MHz • Mode : WFM • Filter : 230.0 kHz • Set an SSG as : Mode : FM Level : 1.0 µV* (–47 dBm) Modulation : 1 kHz Deviation : 75 kHz • Receiving	Rear Panel	Connect a distortion meter to the [EXT SP] jack with an 8 Ω dummy load.	Minimum distortion level	RF	L106
NOISE BLANKER	1	• Display freq. : 149.97000 MHz • Mode : USB • Filter : 3.0 kHz • NB : ON • Apply the following noise signal to the [ANT] connector.  • Receiving	Rear Panel	Connect an oscilloscope to the [EXT SP] jack with an 8 Ω dummy load.	Minimum noise level	RF	L107

*This output level of a standard signal generator (SSG) is indicated as SSG's open circuit.


DC power supply
13.8 V / 1.0 A
to DC 13.8 V
External speaker
Standard signal
generator
0.01–1500 MHz
–17 to –125 dBm
0.13 μV to 32 mV
AC milivoltmeter,
distortion meter,
or oscilloscope
to external speaker jack
to antenna connector
Computer
to RS-232C port
L107
Noise Blanker
adjustment
L106
WFM receiving
adjustment
R521
Total gain
adjustment
L112
R523
Total gain
adjustment

5-4 SOFTWARE ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	OPERATION
REFERENCE FREQUENCY	1	• Click adjustment item [Xtal] on the Adjustment Panel. • Connect a frequency counter to check point CP4 on the RF unit **(see page 5-4)**.	• Click "▲" or "▼" to set reference frequency to 10.250000 MHz.
TUNED BPF	1	• Click adjustment item [BPFtune] on the Adjustment Panel. • Select "BPF 4-1" at the left side of Adjustment Panel. • Manual/Auto Tune : Manual • Set an SSG as : Frequency : 50.02 MHz Level : 50 μV* (–73 dBm) Modulation : OFF • Receiving	• Move the scroll bar at the bottom side of Adjustment Panel, and set maximum S-meter level on the Control Panel. • Then, click "Write" switch to store into memory.
	2	• Same operation as step 1 for the listed frequencies. BPF 4-2 – 58.28 MHz BPF 4-3 – 58.32 MHz BPF 4-4 – 88.02 MHz BPF 4-5 – 108.28 MHz BPF 4-6 – 108.32 MHz BPF 4-7 – 130.02 MHz BPF 4-8 – 149.98 MHz BPF 5-1 – 150.02 MHz BPF 5-2 – 183.28 MHz BPF 5-3 – 183.32 MHz BPF 5-4 – 216.02 MHz BPF 5-5 – 265.68 MHz BPF 5-6 – 265.72 MHz BPF 5-7 – 300.02 MHz BPF 5-8 – 349.98 MHz BPF 6-1 – 350.02 MHz BPF 6-2 – 383.28 MHz BPF 6-3 – 383.32 MHz BPF 6-4 – 433.32 MHz BPF 6-5 – 483.28 MHz BPF 6-6 – 483.32 MHz BPF 6-7 – 558.32 MHz BPF 6-8 – 633.28 MHz BPF 6-9 – 633.32 MHz BPF 6-10 – 699.98 MHz BPF 7-1 – 700.02 MHz BPF 7-2 – 750.02 MHz BPF 7-3 – 799.98 MHz BPF 7-4 – 800.02 MHz BPF 7-5 – 916.68 MHz BPF 7-6 – 916.72 MHz BPF 7-7 – 1016.68 MHz BPF 7-8 – 1016.72 MHz BPF 7-9 – 1166.68 MHz BPF 7-10 – 1166.72 MHz BPF 7-11 – 1299.98 MHz • Receiving	
S-METER	1	• Click adjustment item [Smeter] on the Adjustment Panel. • Select "FM S0" at the left side of Adjustment Panel. • Set an SSG as : Frequency : 149.97000 MHz Mode : FM Level : 0.5 μV* (–113 dBm) Modulation : OFF • Receiving	• Click "Write" switch to store sampled data into memory.
	2	• Same operation as step 1 for the listed levels. • Set an SSG as: FM S3 : 1.3 μV* (–105 dBm) FM S5 : 3.2 μV* (–97 dBm) FM S7 : 13 μV* (–85 dBm) FM S9 : 50 μV* (–73 dBm) FM S9+20 : 280 μV* (–58 dBm) FM S9+40 : 1.6 mV* (–43 dBm) FM S9+60 : 8.9 mV* (–28 dBm) WFM S0 : 0.79 μV* (–109 dBm) WFM S3 : 1.6 μV* (–103 dBm) WFM S5 : 3.2 μV* (–97 dBm) WFM S7 : 13 μV* (–85 dBm) WFM S9 : 50 μV* (–73 dBm) WFM S9+20 : 280 μV* (–58 dBm) WFM S9+40 : 1.6 mV* (–43 dBm) WFM S9+60 : 8.9 mV* (–28 dBm) • Receiving	
S-METER FLAT	1	• Click adjustment item [BPF S] on the Adjustment Panel. • Select "BPF0" at the left side of Adjustment Panel. • Set an SSG as : Frequency : 1.02 MHz Level : 50 μV* (–73 dBm) Modulation : OFF • Receiving	• Click "Write" switch to store sampled data into memory.

*This output level of a standard signal generator (SSG) is indicated as SSG's open circuit.

SOFTWARE ADJUSTMENT (continued)

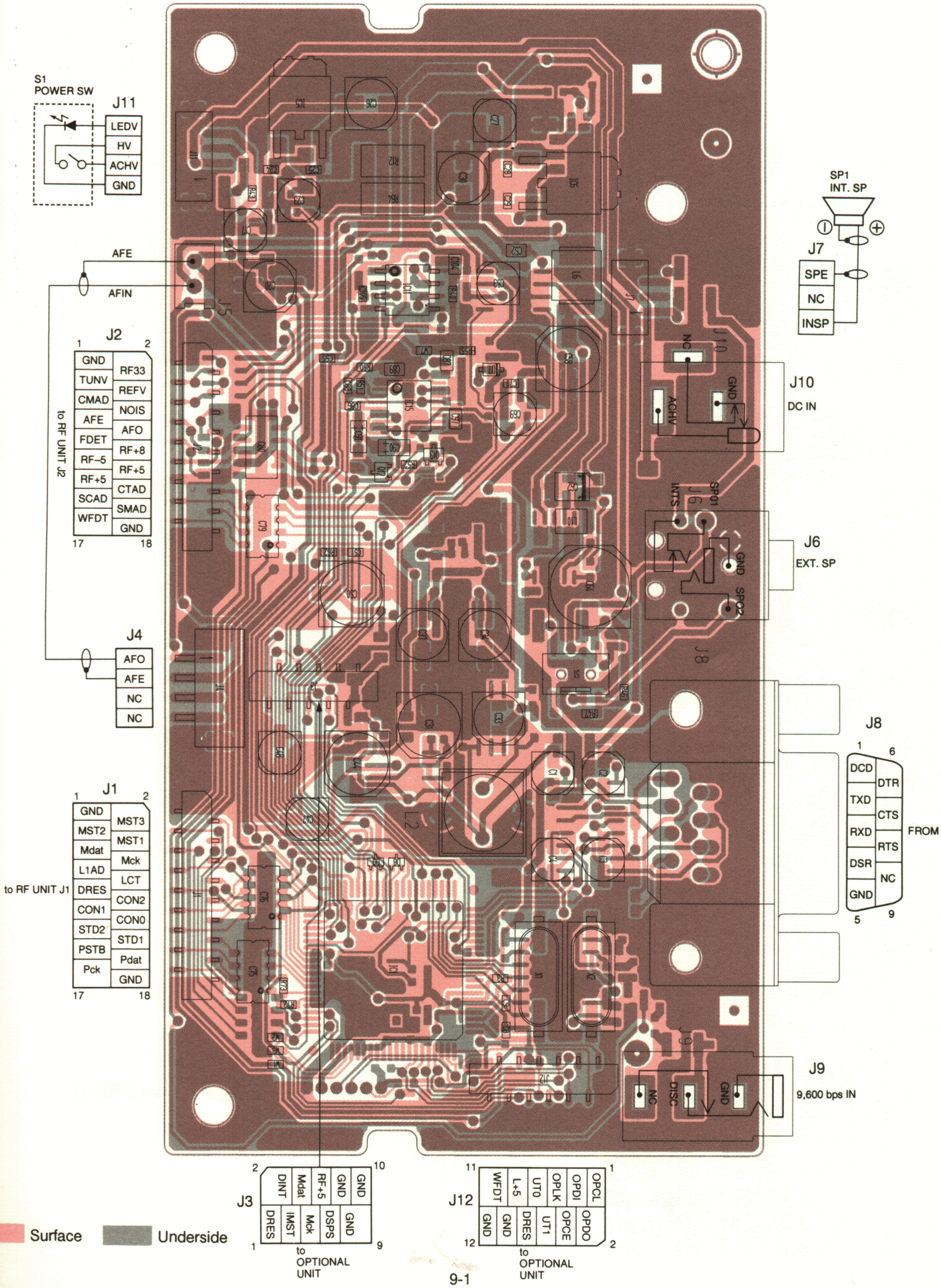
ADJUSTMENT		ADJUSTMENT CONDITION	OPERATION
S-METER FLAT	2	• Same adjustment as step 1 for the listed BPFs frequencies. BPF 1 – 7.02 MHz BPF 2 – 21.02 MHz BPF 3 – 40.02 MHz BPF 4-1 – 50.02 MHz BPF 4-2 – 58.28 MHz BPF 4-3 – 58.32 MHz BPF 4-4 – 88.02 MHz BPF 4-5 – 108.28 MHz BPF 4-6 – 108.32 MHz BPF 4-7 – 130.02 MHz BPF 4-8 – 149.98 MHz BPF 5-1 – 150.02 MHz BPF 5-2 – 183.28 MHz BPF 5-3 – 183.32 MHz BPF 5-4 – 216.02 MHz BPF 5-5 – 265.68 MHz BPF 5-6 – 265.72 MHz BPF 5-7 – 300.02 MHz BPF 5-8 – 349.98 MHz BPF 6-1 – 350.02 MHz BPF 6-2 – 383.28 MHz BPF 6-3 – 383.32 MHz BPF 6-4 – 433.32 MHz BPF 6-5 – 483.28 MHz BPF 6-6 – 483.32 MHz BPF 6-7 – 558.32 MHz BPF 6-8 – 633.28 MHz BPF 6-9 – 633.32 MHz BPF 6-10 – 699.98 MHz BPF 7-1 – 700.02 MHz BPF 7-2 – 750.02 MHz BPF 7-3 – 799.98 MHz BPF 7-4 – 800.02 MHz BPF 7-5 – 916.68 MHz BPF 7-6 – 916.72 MHz BPF 7-7 – 1016.68 MHz BPF 7-8 – 1016.72 MHz BPF 7-9 – 1166.68 MHz BPF 7-10 – 1166.72 MHz BPF 7-11 – 1299.98 MHz • Receiving	
SCOPE S	1	• Click adjustment item [Scope S] on the Adjustment Panel. • Select "S0" at the left side of Adjustment Panel. • Mode : FM • Filter : 15.0 kHz • Set an SSG as : Frequency : 149.97000 MHz Level : 0.32 μV* (–117 dBm) Modulation : OFF • Receiving	• Click "Write" switch to store sampled data into memory.
	2	• Same operation as step 1 for the listed levels. • Set an SSG as : S3 : 3.2 μV* (–97 dBm) S5 : 10 μV* (–87 dBm) S7 : 32 μV* (–77 dBm) S9 : 100 μV* (–67 dBm) S9+20 : 320 μV* (–57 dBm) S9+40 : 1.0 mV* (–47 dBm) S9+60 : 3.2 mV* (–37 dBm) • Receiving	
CENTER INDICATOR	1	• Click adjustment item [Center] on the Adjustment Panel. • Select "CW low" at the left side of Adjustment Panel. • Set an SSG as : Frequency : 149.96700 MHz Level : 50 μV* (–73 dBm) Modulation : OFF • Receiving	• Click "Write" switch to store sampled data into memory.
	2	• Select "CW high" at the left side of Adjustment Panel. • Set an SSG as : Frequency : 149.97300 MHz • Receiving	• Click "Write" switch to store sampled data into memory.
NOISE SQUELCH	1	• Click adjustment item [Noise SQL] on the Adjustment Panel.	• Click each "Write" switch for Timing and Level.
	2	• Set an Adjustment panel as: Timing : T2 — 2 T3 — 100 Level : Thresh — 20 Tight — 20	• Click "▼" then "Write" switches at 'Level' to set Thresh/Tight data until noise disappears. **NOTE**: "Write" switch must be clicked at each level, otherwise the level is invalid.
	3	• Set an Adjustment panel as: Timing : T2 — 2 T3 — 4	• Click "Write" switch for Timing.

*This output level of a standard signal generator (SSG) is indicated as SSG's open circuit.

9-1 LOGIC UNIT

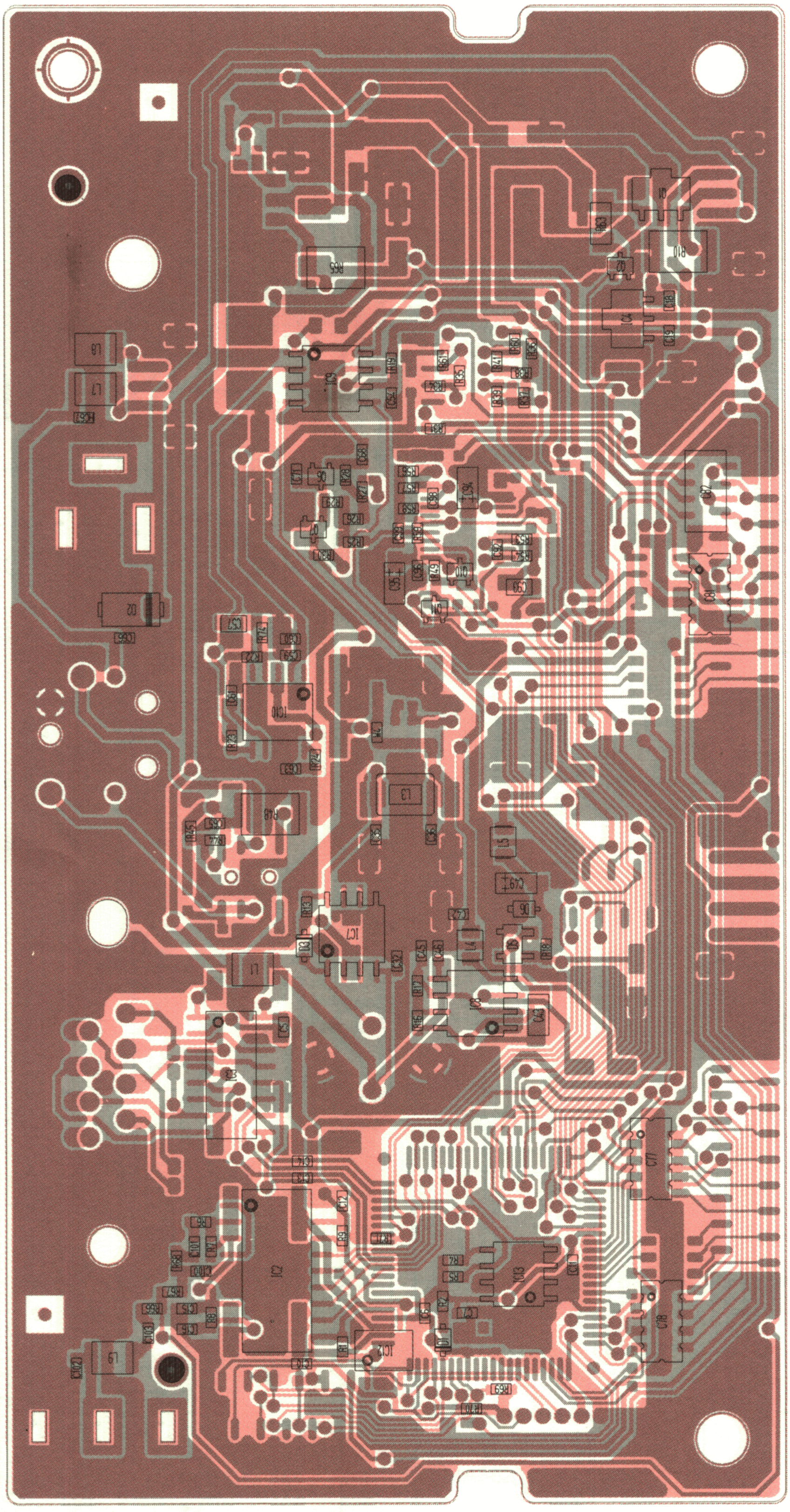
• TOP VIEW

The combination of this page and the next page shows the unit layout in the same configuration as the actual P.C. Board.



Surface Underside

• **BOTTOM VIEW**



Surface Underside

F UNIT

TOP VIEW

to LOGIC UNIT J1

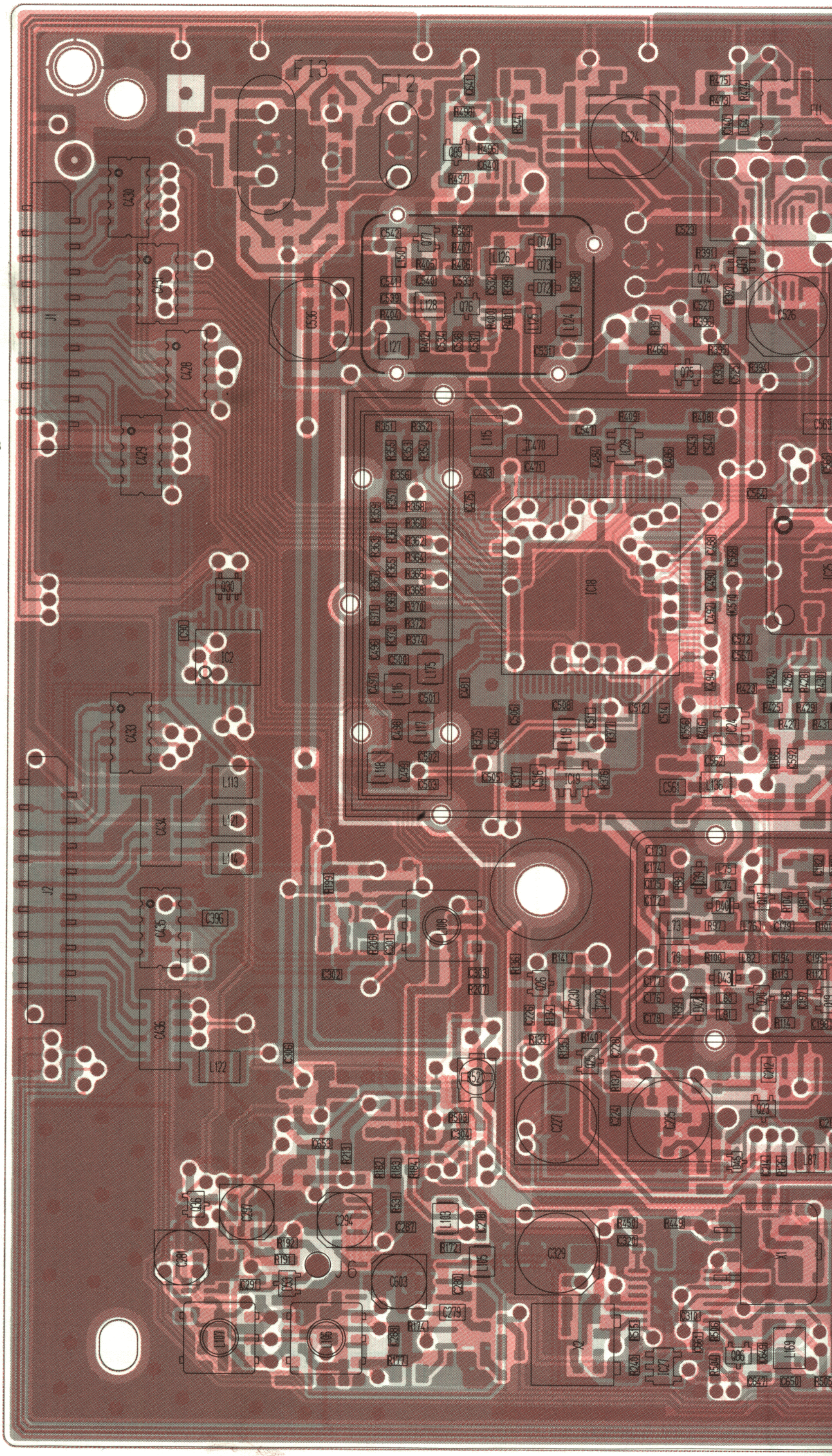
J1

1	2
GND	Pck
Pdat	PSTB
STD1	STD2
CON0	CON1
CON2	DRES
LCT	L1AD
Mck	Mdat
MST1	MST2
MST3	GND
17	18

to LOGIC UNIT J2

J2

1	2
GND	WFDT
SMAD	SCAD
CTAD	RF+5
RF+5	RF−5
RF+8	FDET
AFO	AFE
NOIS	CMAD
REFV	TUNV
RF33	GND
17	18



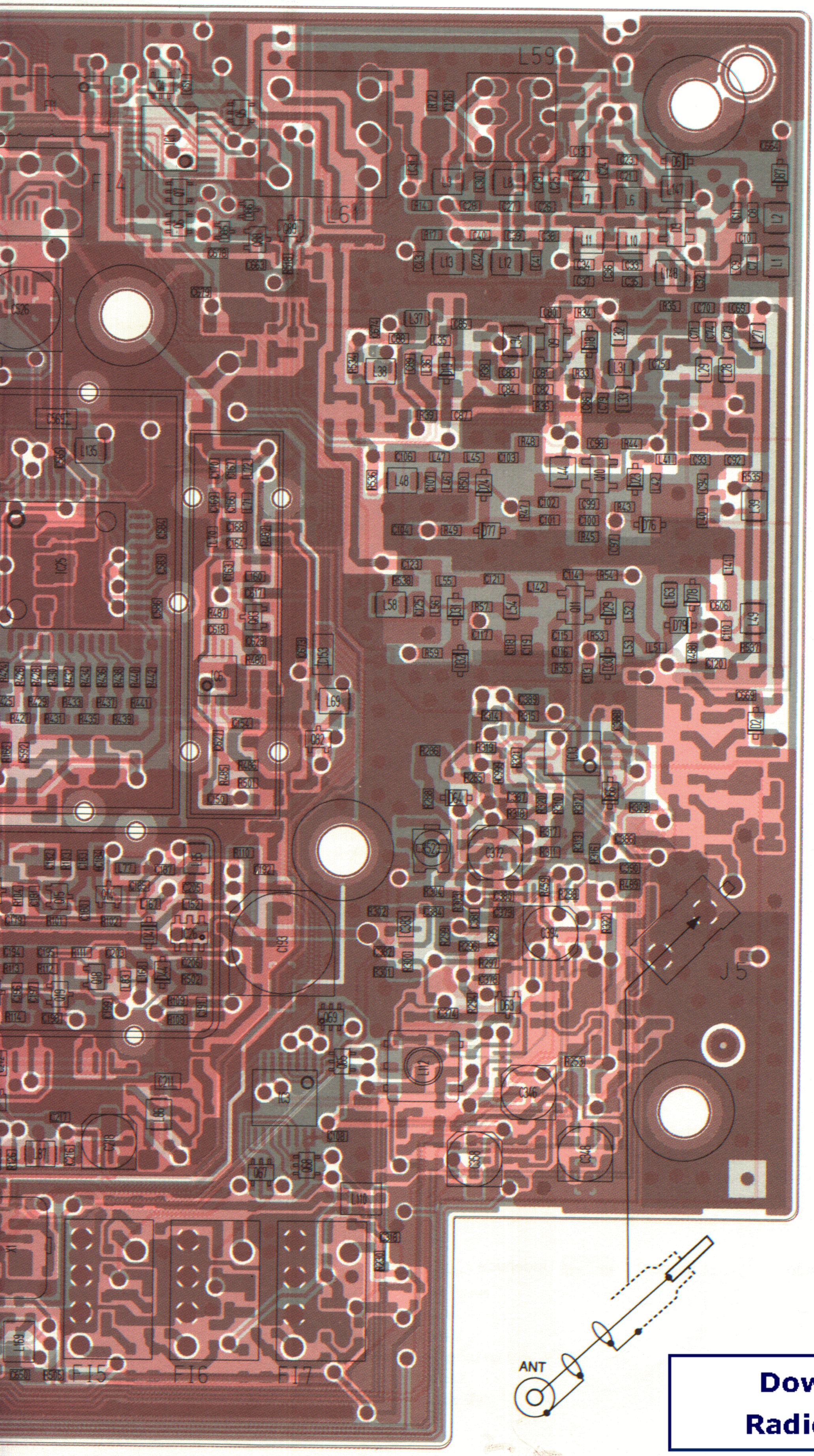
Surface

Inside-1

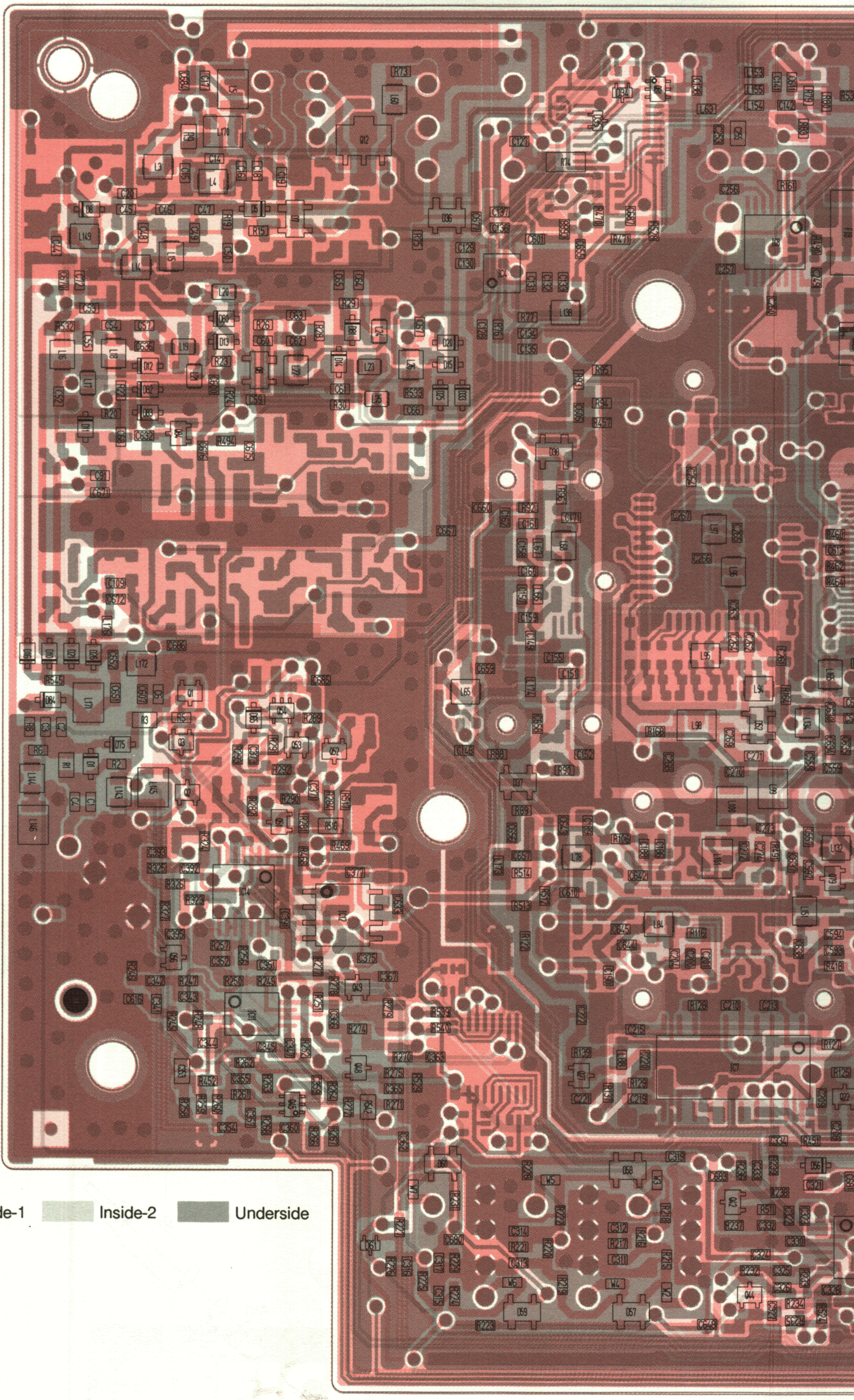
Inside-2

Underside

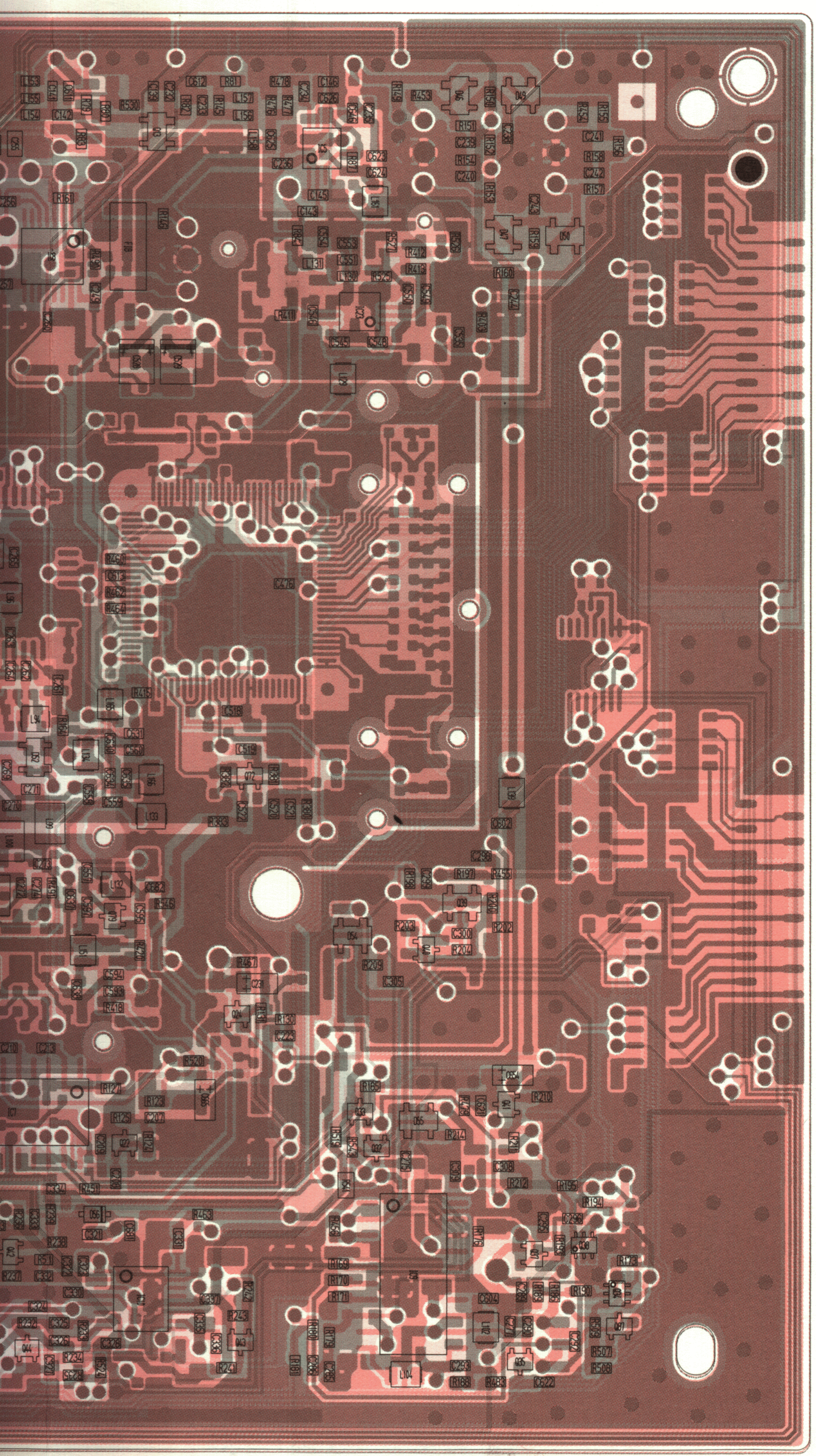
The combination of this page and the next page shows the unit layout in the same configuration as the actual P.C. Board.

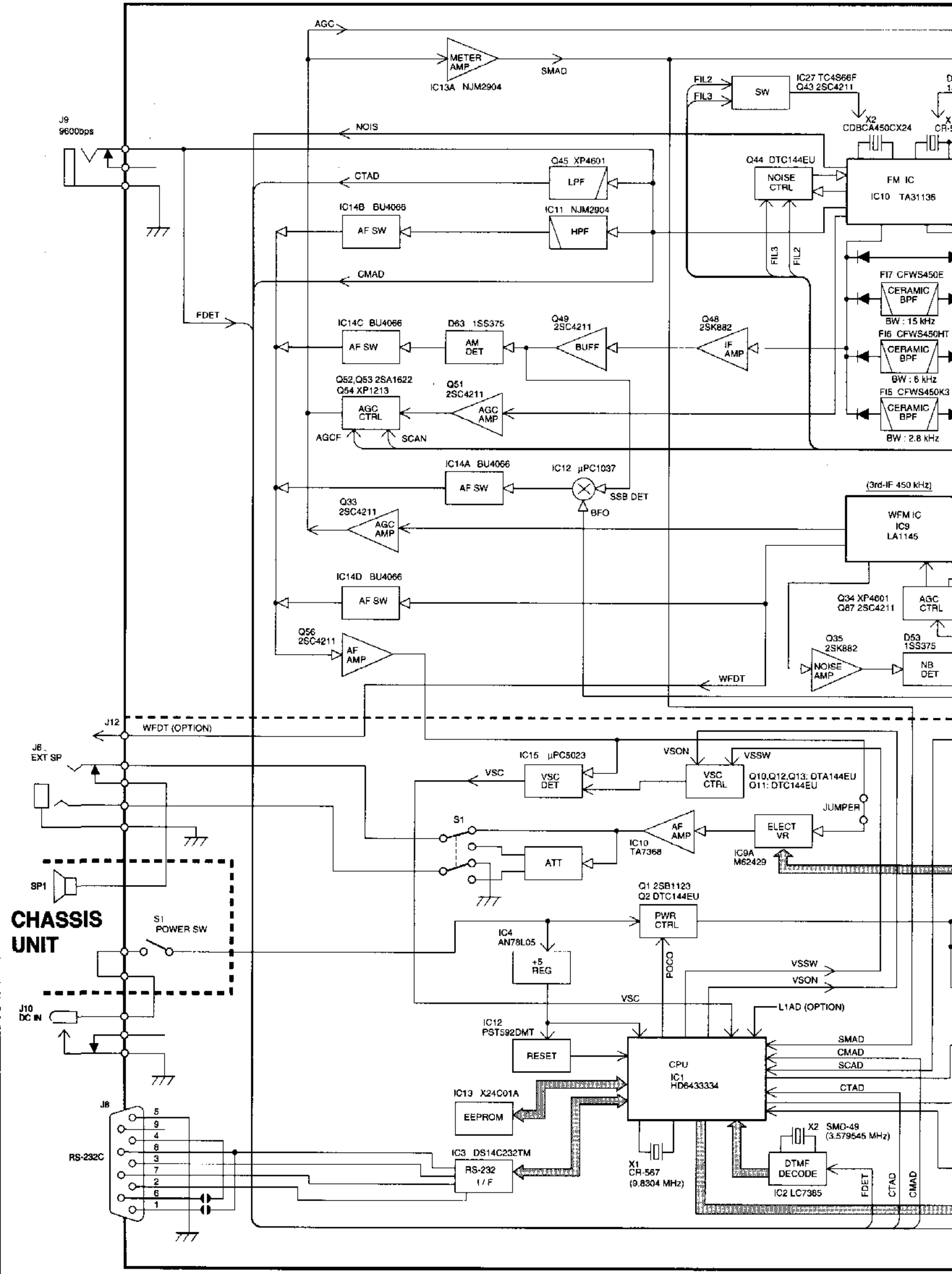


BOTTOM VIEW

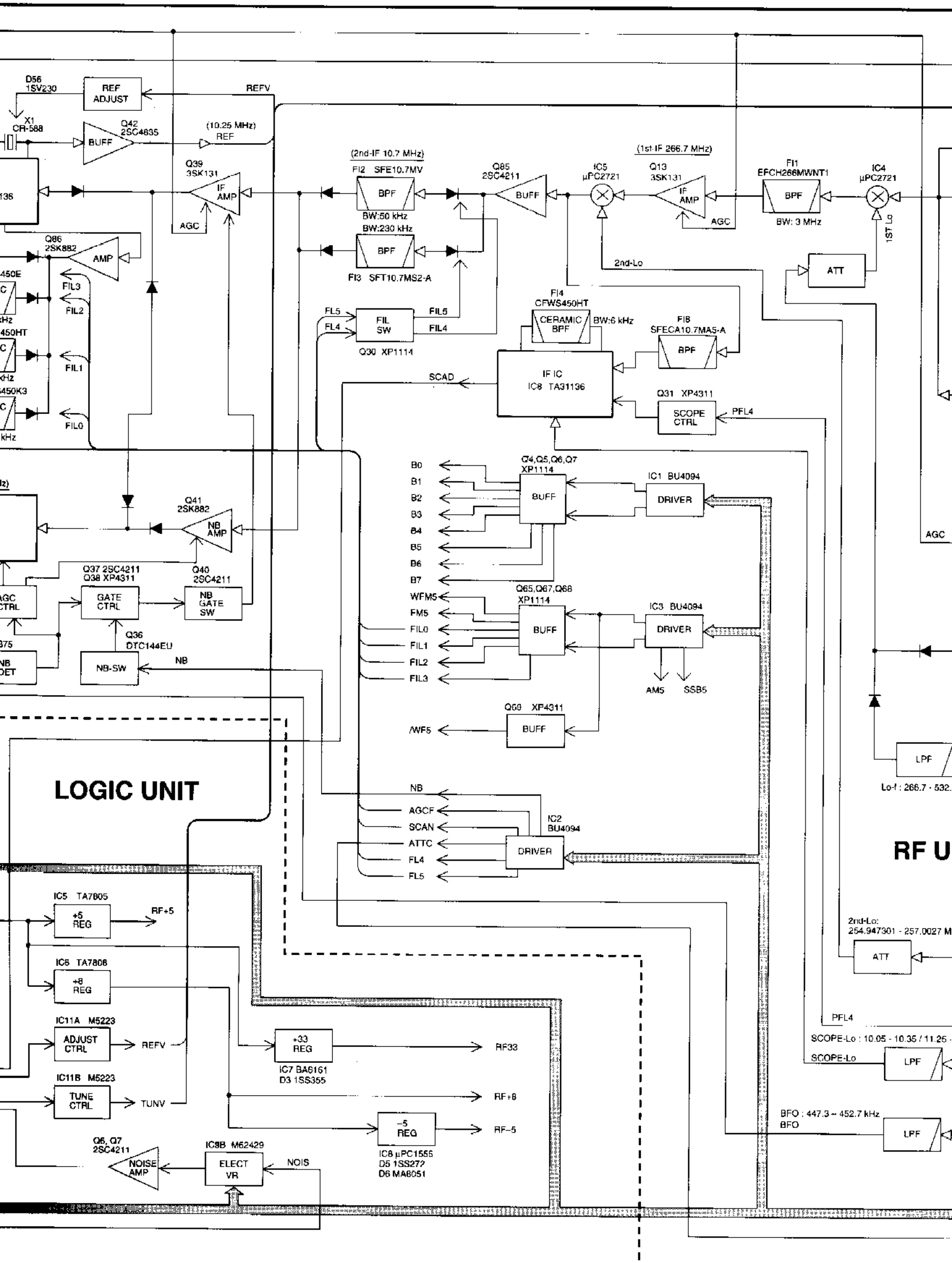


Surface Inside-1 Inside-2 Underside

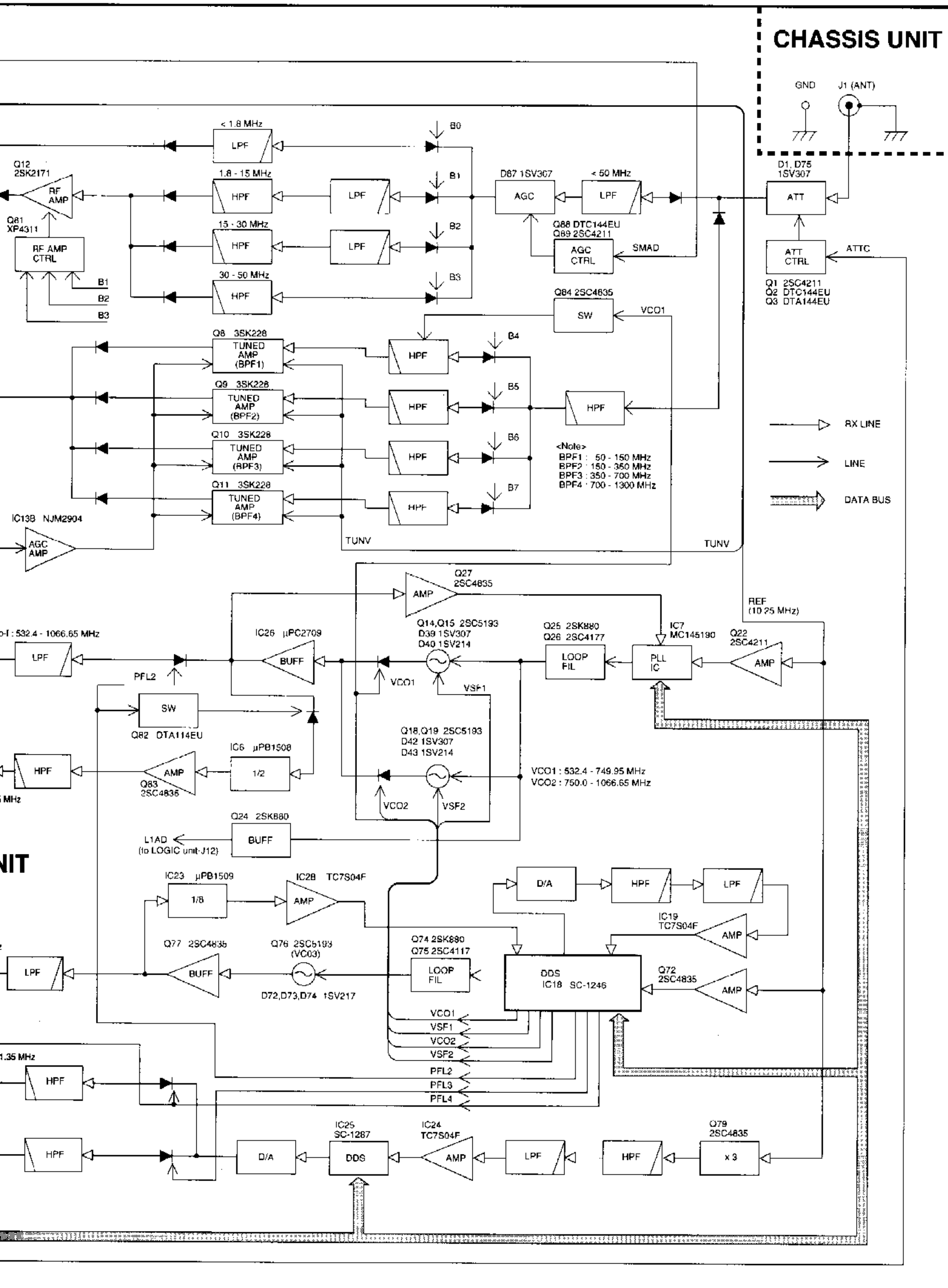




AGC
METER AMP
IC13A NJM2904
SMAD
FIL2
FIL3
SW
IC27 TC4S66F
Q43 2SC4211
X2
CDBCA450CX24
J9
9600bps
NOIS
Q44 DTC144EU
NOISE CTRL
FM IC
IC10 TA31136
Q45 XP4601
LPF
CTAD
IC14B BU4066
AF SW
IC11 NJM2904
HPF
FIL3
FIL2
FI7 CFWS450E
CERAMIC BPF
BW : 15 kHz
CMAD
FDET
IC14C BU4066
AF SW
D63 1SS375
AM DET
Q49 2SC4211
BUFF
Q48 2SK882
IF AMP
FI6 CFWS450HT
CERAMIC BPF
BW : 6 kHz
Q52,Q53 2SA1622
Q54 XP1213
AGC CTRL
Q51 2SC4211
AGC AMP
FI5 CFWS450K3
CERAMIC BPF
BW : 2.8 kHz
AGCF
SCAN
IC14A BU4066
AF SW
IC12 µPC1037
SSB DET
BFO
(3rd-IF 450 kHz)
WFM IC
IC9
LA1145
Q33 2SC4211
AGC AMP
IC14D BU4066
AF SW
Q34 XP4601
Q87 2SC4211
AGC CTRL
Q56 2SC4211
AF AMP
Q35 2SK882
NOISE AMP
D53 1SS375
NB DET
WFDT
J12
WFDT (OPTION)
J6
EXT SP
IC15 µPC5023
VSC
VSC DET
VSON
VSC CTRL
VSSW
Q10,Q12,Q13: DTA144EU
Q11: DTC144EU
JUMPER
S1
AF AMP
IC10 TA7368
ELECT VR
IC9A M62429
ATT
SP1
CHASSIS UNIT
S1 POWER SW
Q1 2SB1123
Q2 DTC144EU
PWR CTRL
IC4 AN78L05
+5 REG
POCO
VSSW
VSON
VSC
L1AD (OPTION)
J10 DC IN
IC12 PST592DMT
RESET
CPU
IC1 HD6433334
SMAD
CMAD
SCAD
CTAD
IC13 X24C01A
EEPROM
J8
RS-232C
5 9 4 8 3 7 2 6 1
IC3 DS14C232TM
RS-232 I/F
X1 CR-567 (9.8304 MHz)
X2 SMD-49 (3.579545 MHz)
DTMF DECODE
IC2 LC7385
FDET
CTAD
CMAD

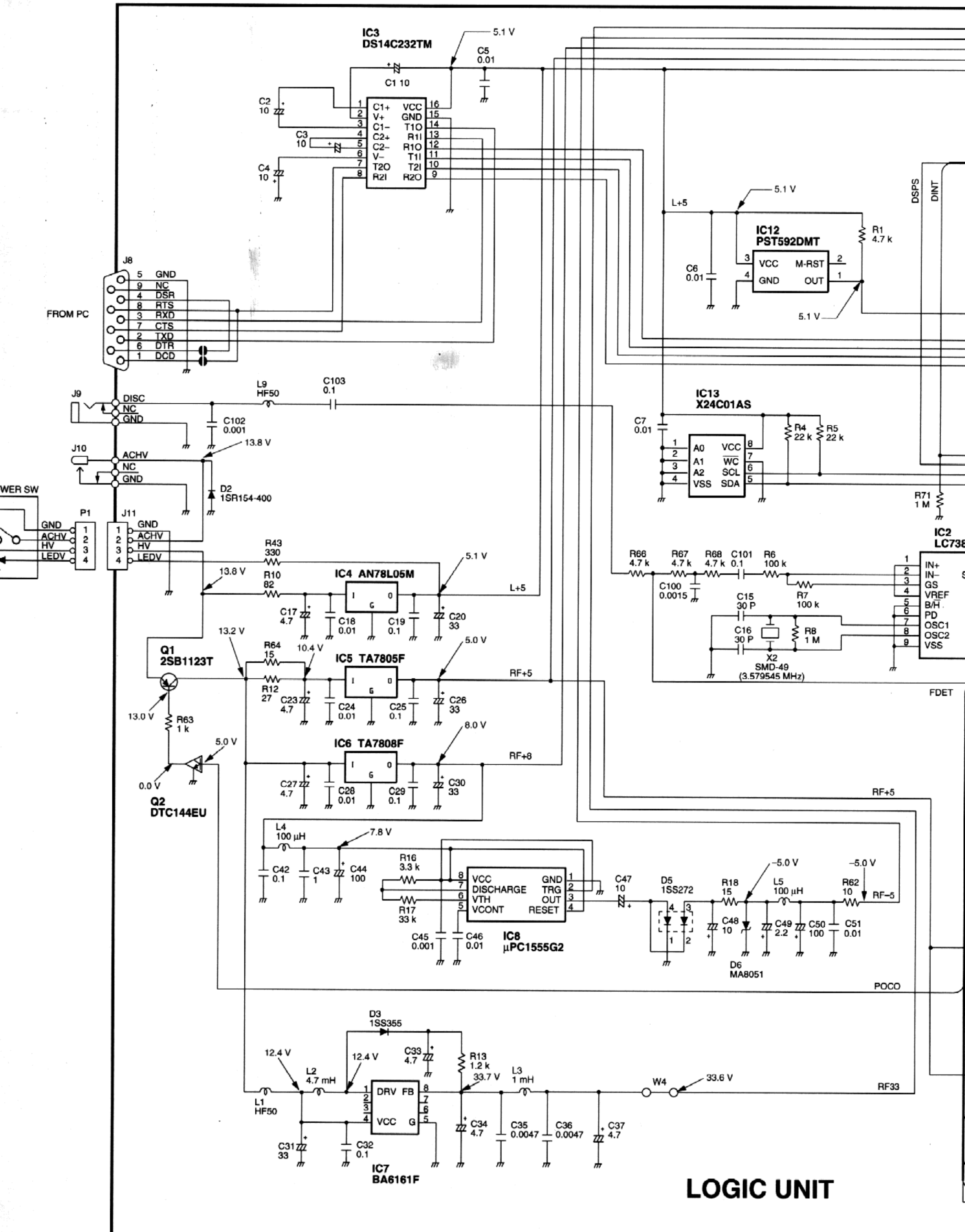


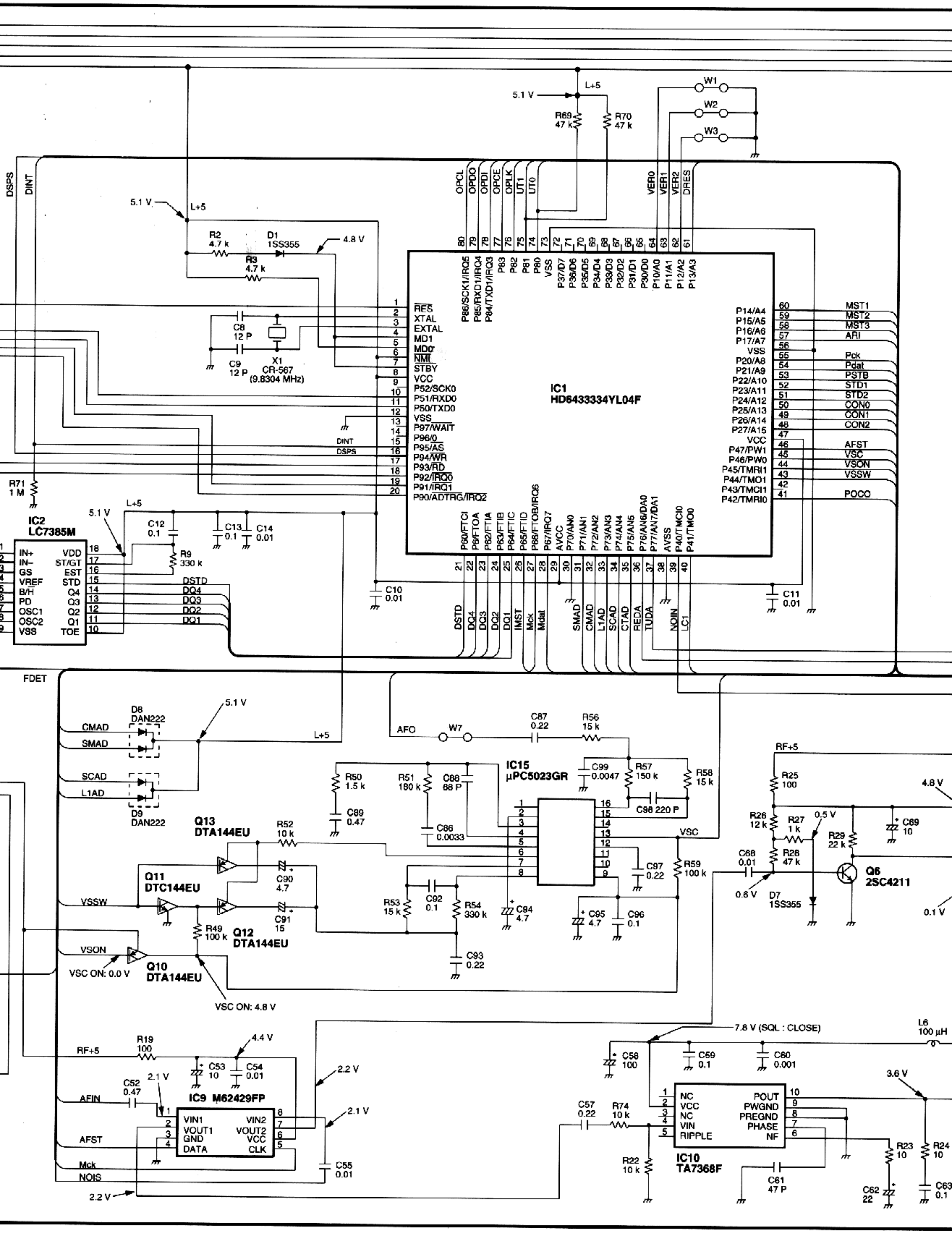
LOGIC UNIT
RF U
D56 1SV230
REF ADJUST
REFV
X1 CR-588
BUFF
Q42 2SC4835
(10.25 MHz) REF
Q39 3SK131
IF AMP
AGC
(2nd-IF 10.7 MHz)
FI2 SFE10.7MV
BPF
BW:50 kHz
BW:230 kHz
FI3 SFT10.7MS2-A
Q85 2SC4211
IC5 μPC2721
(1st-IF 266.7 MHz)
Q13 3SK131
FI1 EFCH266MWNT1
BW: 3 MHz
IC4 μPC2721
1ST Lo
2nd-Lo
ATT
Q86 2SK882
AMP
FIL3
FIL2
FIL1
FIL0
450E
450HT
450K3
FL5
FL4
FIL SW
Q30 XP1114
FI4 CFWS450HT
CERAMIC BPF
BW:6 kHz
FI8 SFECA10.7MA5-A
SCAD
IF IC
IC8 TA31136
Q31 XP4311
SCOPE CTRL
PFL4
B0
B1
B2
B3
B4
B5
B6
B7
Q4,Q5,Q6,Q7 XP1114
IC1 BU4094
DRIVER
Q41 2SK882
NB AMP
Q37 2SC4211
Q38 XP4311
GATE CTRL
Q40 2SC4211
NB GATE SW
AGC CTRL
Q36 DTC144EU
NB-SW
NB
NB DET
WFM5
FM5
FIL0
FIL1
FIL2
FIL3
Q65,Q67,Q68 XP1114
IC3 BU4094
AM5
SSB5
Q69 XP4311
/WF5
AGC
LPF
Lo-f : 266.7 - 532.
NB
AGCF
SCAN
ATTC
FL4
FL5
IC2 BU4094
IC5 TA7805
+5 REG
RF+5
IC6 TA7808
+8 REG
IC11A M5223
ADJUST CTRL
REFV
IC11B M5223
TUNE CTRL
TUNV
+33 REG
IC7 BA6161
D3 1SS355
RF33
RF+8
-5 REG
RF-5
IC8 μPC1555
D5 1SS272
D6 MA8051
Q6, Q7 2SC4211
NOISE AMP
IC9B M62429
ELECT VR
NOIS
2nd-Lo: 254.947301 - 257.0027 M
PFL4
SCOPE-Lo : 10.05 - 10.35 / 11.25 -
SCOPE-Lo
BFO : 447.3 ~ 452.7 kHz
BFO

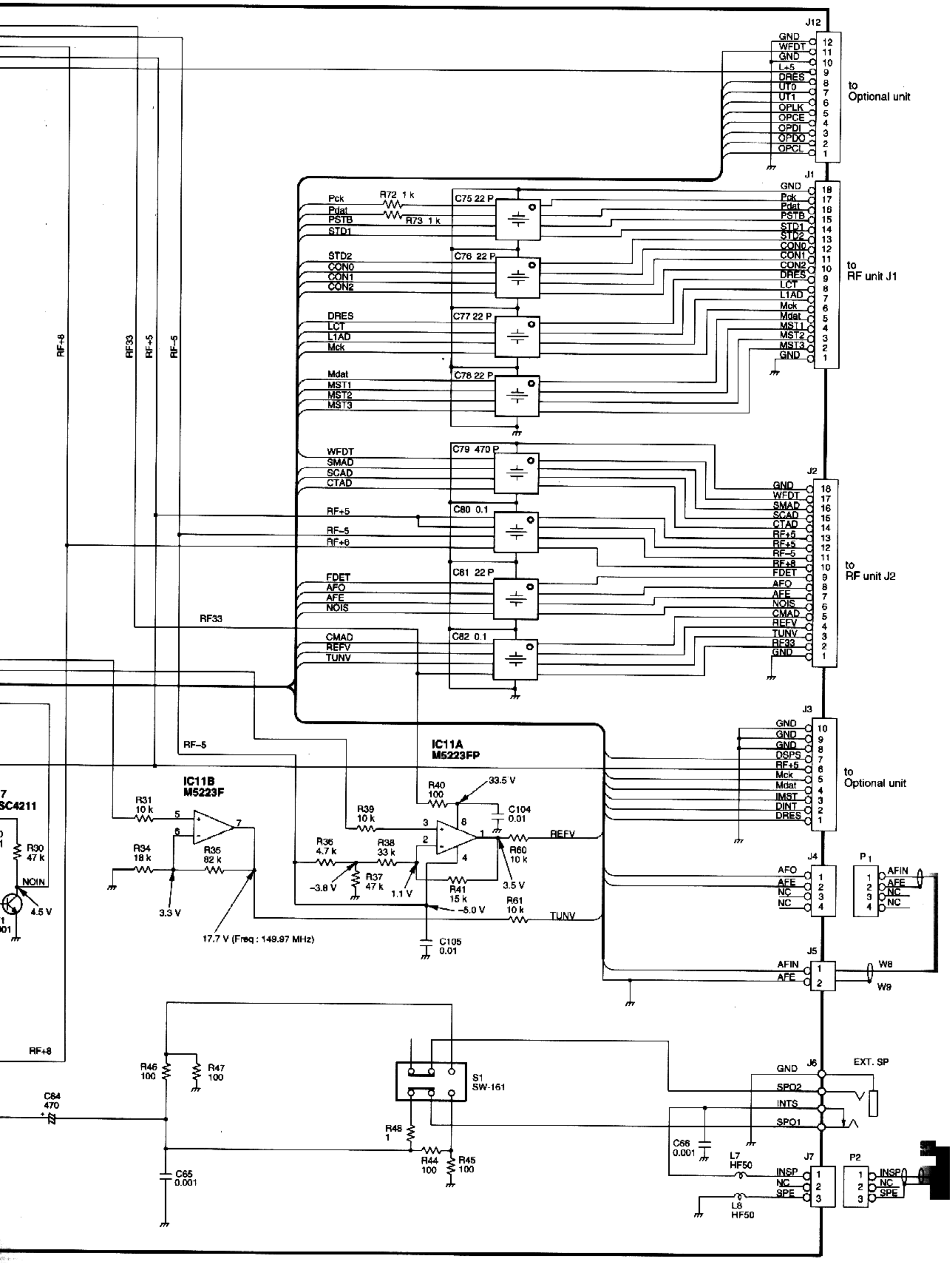


CHASSIS UNIT
GND
J1 (ANT)
D1, D75
1SV307
ATT
ATT CTRL
ATTC
Q1 2SC4211
Q2 DTC144EU
Q3 DTA144EU
D87 1SV307
AGC
< 50 MHz
LPF
Q88 DTC144EU
Q89 2SC4211
AGC CTRL
SMAD
< 1.8 MHz
LPF
B0
1.8 - 15 MHz
HPF
LPF
B1
15 - 30 MHz
HPF
LPF
B2
30 - 50 MHz
HPF
B3
Q12
2SK2171
RF AMP
Q81
XP4311
RF AMP CTRL
B1
B2
B3
Q84 2SC4835
SW
VCO1
Q8 3SK228
TUNED AMP (BPF1)
Q9 3SK228
TUNED AMP (BPF2)
Q10 3SK228
TUNED AMP (BPF3)
Q11 3SK228
TUNED AMP (BPF4)
HPF
B4
HPF
B5
HPF
HPF
B6
HPF
B7
<Note>
BPF1 : 50 - 150 MHz
BPF2 : 150 - 350 MHz
BPF3 : 350 - 700 MHz
BPF4 : 700 - 1300 MHz
RX LINE
LINE
DATA BUS
IC13B NJM2904
AGC AMP
TUNV
TUNV
Q27
2SC4835
AMP
REF
(10.25 MHz)
o-f : 532.4 - 1066.65 MHz
LPF
IC26 µPC2709
BUFF
Q14,Q15 2SC5193
D39 1SV307
D40 1SV214
Q25 2SK880
Q26 2SC4177
LOOP FIL
IC7
MC145190
PLL IC
Q22
2SC4211
AMP
PFL2
SW
Q82 DTA114EU
VCO1
VSF1
Q18,Q19 2SC5193
D42 1SV307
D43 1SV214
IC6 µPB1508
1/2
HPF
AMP
Q83
2SC4835
5 MHz
VCO1 : 532.4 - 749.95 MHz
VCO2 : 750.0 - 1066.65 MHz
VCO2
VSF2
Q24 2SK880
BUFF
L1AD
(to LOGIC unit-J12)
NIT
IC23 µPB1509
1/8
IC28 TC7S04F
AMP
D/A
HPF
LPF
IC19
TC7S04F
AMP
Q77 2SC4835
Q76 2SC5193
(VC03)
Q74 2SK880
Q75 2SC4117
LOOP FIL
LPF
BUFF
D72,D73,D74 1SV217
DDS
IC18 SC-1246
Q72
2SC4835
AMP
VCO1
VSF1
VCO2
VSF2
PFL2
PFL3
PFL4
1.35 MHz
HPF
HPF
D/A
IC25
SC-1287
DDS
IC24
TC7S04F
AMP
LPF
HPF
Q79
2SC4835
x 3

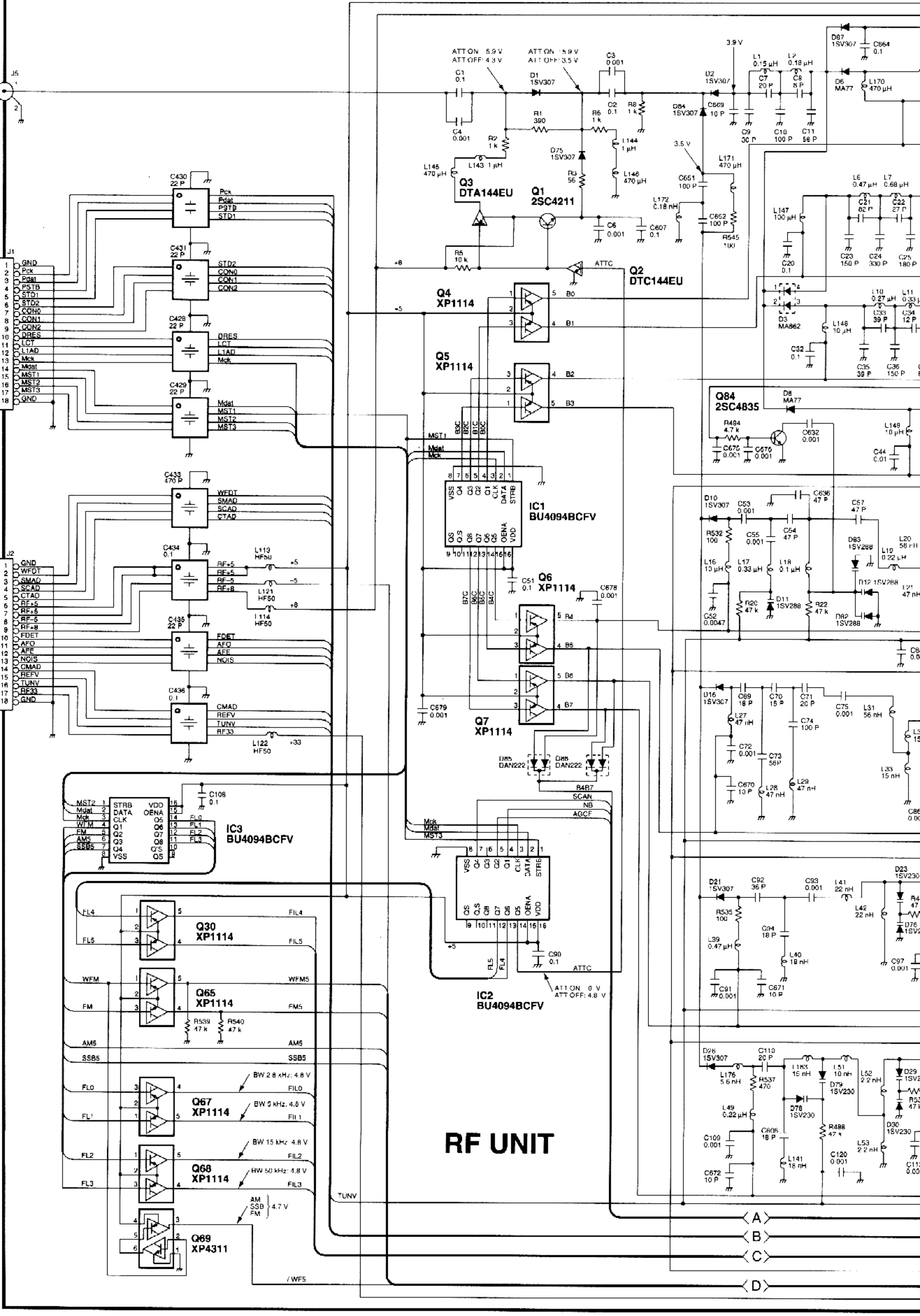
SECTION 11 VOLTAGE DIAGRAM

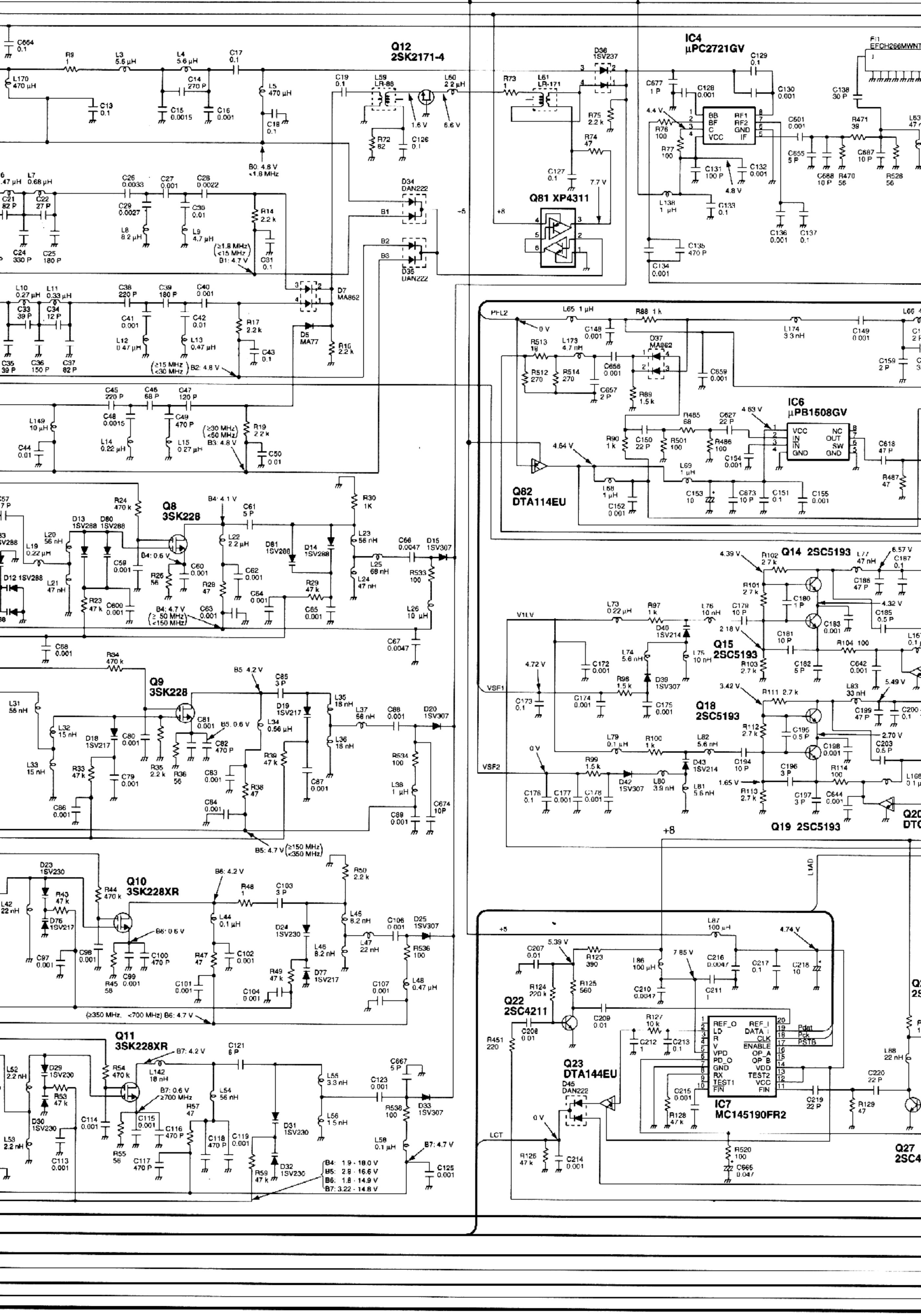



IC1
HD6433334YL04F
IC2
LC7385M
IC15
µPC5023GR
IC9 M62429FP
IC10
TA7368F
Q13
DTA144EU
Q11
DTC144EU
Q12
DTA144EU
Q10
DTA144EU
Q6
2SC4211
D1
1SS355
D7
1SS355
D8
DAN222
D9
DAN222
X1
CR-567
(9.8304 MHz)
5.1 V
L+5
4.8 V
4.4 V
2.2 V
2.1 V
3.6 V
0.5 V
0.6 V
0.1 V
7.8 V (SQL : CLOSE)
VSC ON: 0.0 V
VSC ON: 4.8 V
RF+5
W1
W2
W3
W7
AFO
DSPS
DINT
FDET
CMAD
SMAD
SCAD
L1AD
VSSW
VSON
AFIN
AFST
Mck
NOIS
VSC
MST1
MST2
MST3
ARI
Pck
Pdat
PSTB
STD1
STD2
CON0
CON1
CON2
AFST
VSC
VSON
VSSW
POCO
DSTD
DQ4
DQ3
DQ2
DQ1
IMST
Mck
Mdat
SMAD
CMAD
L1AD
SCAD
CTAD
REDA
TUDA
NOIN
LC1
L6
100 µH

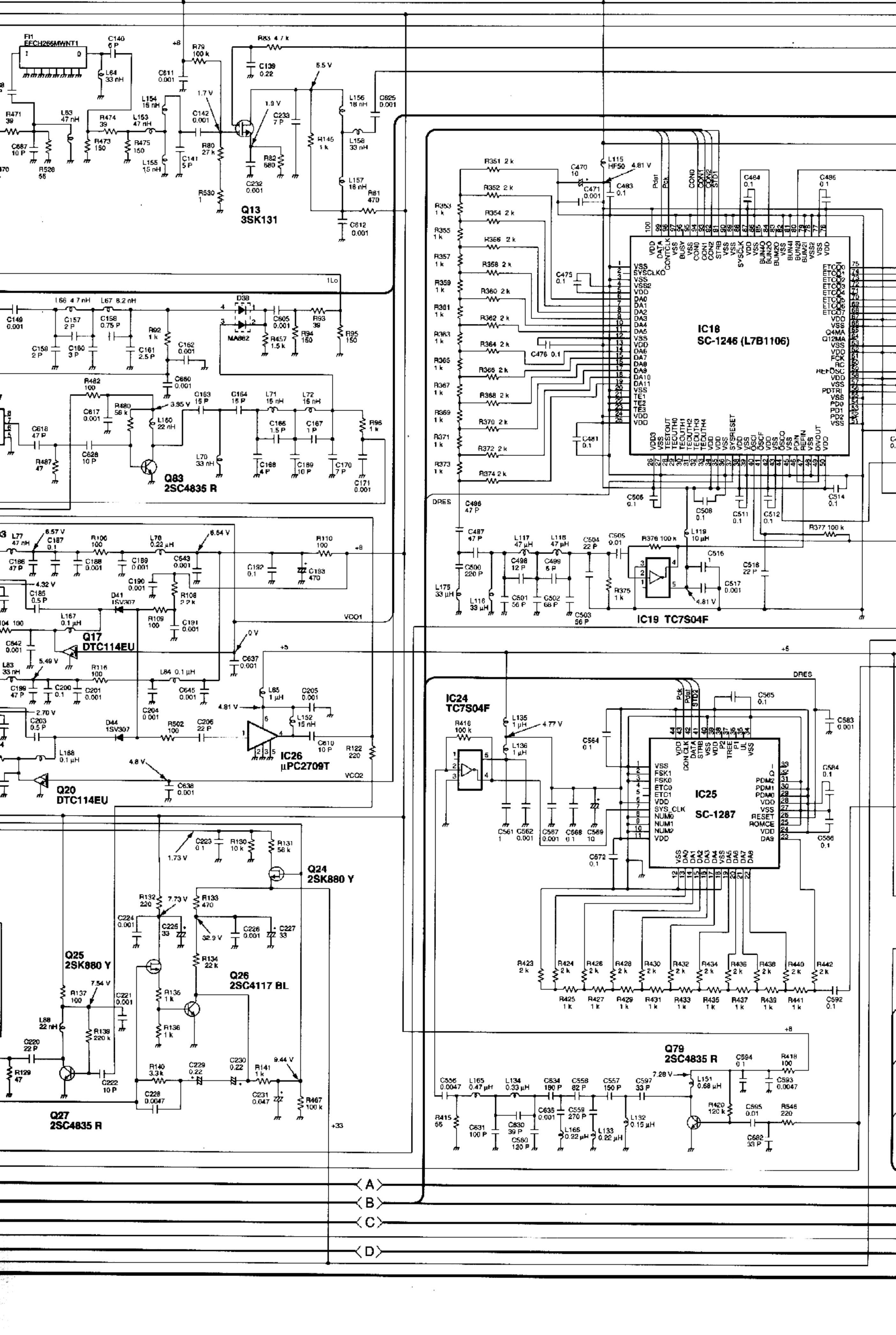


J12
to Optional unit
GND
WFDT
GND
L+5
DRES
UT0
UT1
OPLK
OPCE
OPDI
OPDO
OPCL
J1
to RF unit J1
Pck
Pdat
PSTB
STD1
STD2
CON0
CON1
CON2
DRES
LCT
L1AD
Mck
Mdat
MST1
MST2
MST3
R72 1 k
R73 1 k
C75 22 P
C76 22 P
C77 22 P
C78 22 P
C79 470 P
C80 0.1
C81 22 P
C82 0.1
J2
to RF unit J2
WFDT
SMAD
SCAD
CTAD
RF+5
RF–5
RF+8
FDET
AFO
AFE
NOIS
CMAD
REFV
TUNV
RF33
RF+8
RF33
RF+5
RF–5
J3
to Optional unit
DSPS
Mck
Mdat
IMST
DINT
IC11A
M5223FP
IC11B
M5223F
SC4211
R30 47 k
NOIN
4.5 V
R31 10 k
R34 18 k
R35 82 k
3.3 V
17.7 V (Freq : 149.97 MHz)
R36 4.7 k
R37 47 k
R38 33 k
R39 10 k
R40 100
R41 15 k
R60 10 k
R61 10 k
33.5 V
C104 0.01
C105 0.01
–3.8 V
1.1 V
3.5 V
–5.0 V
J4
P1
AFIN
NC
J5
W8
W9
J6
EXT. SP
SPO2
INTS
SPO1
S1
SW-161
R46 100
R47 100
R48 1
R44 100
R45 100
C64 470
C65 0.001
C66 0.001
L7 HF50
L8 HF50
J7
P2
INSP
SPE

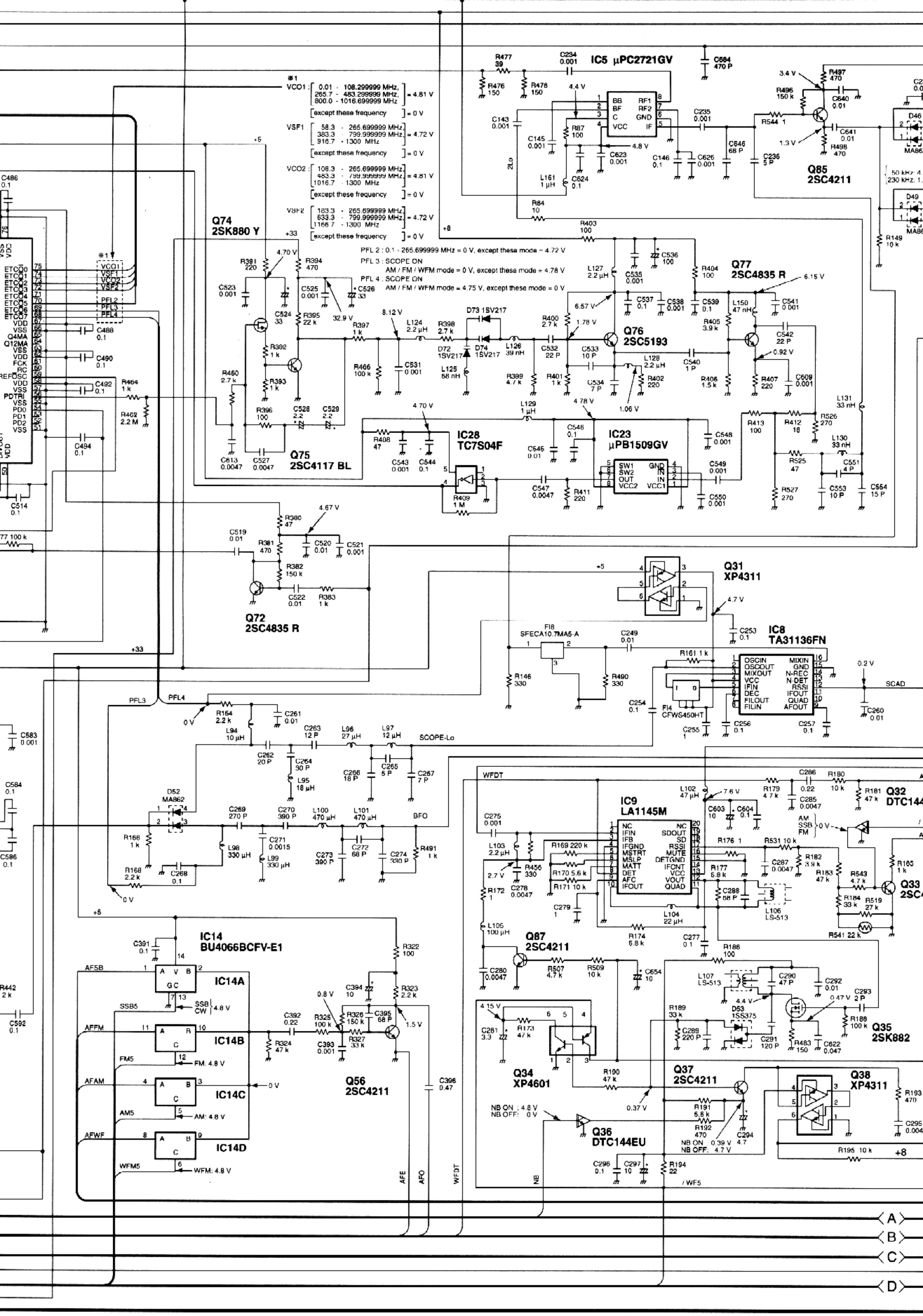

RF UNIT
J5
J1
J2
Q1 2SC4211
Q2 DTC144EU
Q3 DTA144EU
Q4 XP1114
Q5 XP1114
Q6 XP1114
Q7 XP1114
Q84 2SC4835
IC1 BU4094BCFV
IC2 BU4094BCFV
IC3 BU4094BCFV
Q30 XP1114
Q65 XP1114
Q67 XP1114
Q68 XP1114
Q69 XP4311
ATT ON: 5.9 V
ATT OFF: 4.3 V
ATT ON: 5.9 V
ATT OFF: 3.5 V
ATT ON: 0 V
ATT OFF: 4.8 V
BW 2.8 kHz: 4.8 V
BW 5 kHz: 4.8 V
BW 15 kHz: 4.8 V
BW 50 kHz: 4.8 V
AM
SSB
FM
4.7 V
A
B
C
D



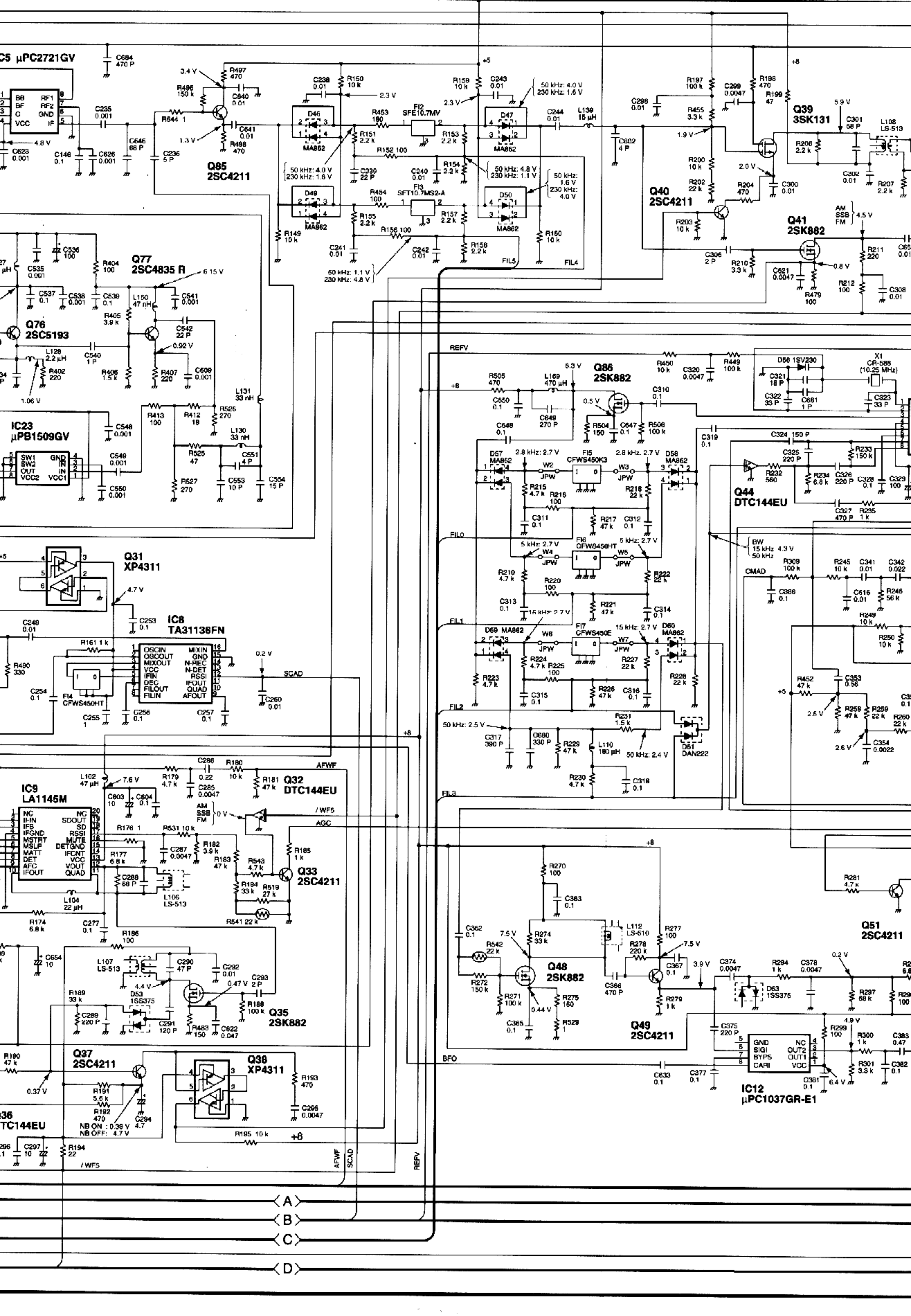
Q12 2SK2171-4
IC4 μPC2721GV
Q81 XP4311
IC6 μPB1508GV
Q82 DTA114EU
Q8 3SK228
Q14 2SC5193
Q15 2SC5193
Q9 3SK228
Q18 2SC5193
Q19 2SC5193
Q10 3SK228XR
Q22 2SC4211
Q23 DTA144EU
IC7 MC145190FR2
Q11 3SK228XR
Q27
B4: 1.9 - 18.0 V
B5: 2.8 - 16.6 V
B6: 1.8 - 14.9 V
B7: 3.22 - 14.8 V



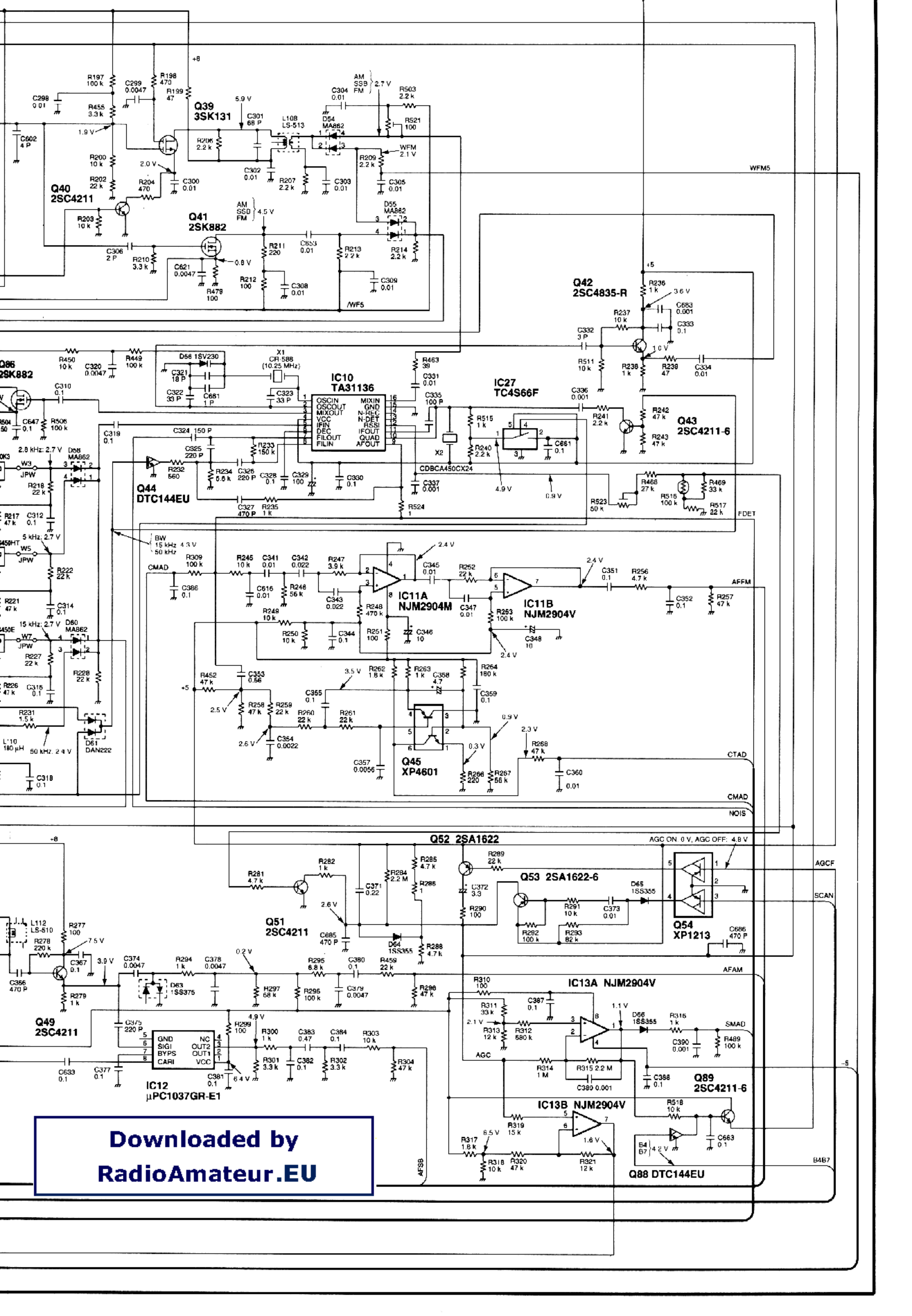
FI1 EFCH266MWNT1
Q13 3SK131
Q83 2SC4835 R
Q17 DTC114EU
Q20 DTC114EU
Q24 2SK880 Y
Q25 2SK880 Y
Q26 2SC4117 BL
Q27 2SC4835 R
Q79 2SC4835 R
D38 MA862
D41 1SV307
D44 1SV307
IC18 SC-1246 (L7B1106)
IC19 TC7S04F
IC24 TC7S04F
IC25 SC-1287
IC26 μPC2709T
VCO1
VCO2
DRES
1Lo
+5
+8
+33
A
B
C
D



IC5 μPC2721GV
Q85 2SC4211
VCO1 : 0.01 - 108.299999 MHz, 265.7 - 483.299999 MHz, 800.0 - 1016.699999 MHz = 4.81 V
except these frequency = 0 V
VSF1 : 58.3 - 265.699999 MHz, 383.3 - 799.999999 MHz, 916.7 - 1300 MHz = 4.72 V
except these frequency = 0 V
VCO2 : 108.3 - 265.699999 MHz, 483.3 - 799.999999 MHz, 1016.7 - 1300 MHz = 4.81 V
except these frequency = 0 V
VSF2 : 183.3 - 265.699999 MHz, 633.3 - 799.999999 MHz, 1166.7 - 1300 MHz = 4.72 V
except these frequency = 0 V
PFL 2 : 0.1 - 265.699999 MHz = 0 V, except these mode = 4.72 V
PFL 3 : SCOPE ON
AM / FM / WFM mode = 0 V, except these mode = 4.78 V
PFL 4 : SCOPE ON
AM / FM / WFM mode = 4.75 V, except these mode = 0 V
Q74 2SK880 Y
Q75 2SC4117 BL
Q76 2SC5193
Q77 2SC4835 R
IC28 TC7S04F
IC23 μPB1509GV
Q72 2SC4835 R
Q31 XP4311
IC8 TA31136FN
FI8 SFECA10.7MA5-A
FI4 CFWS450HT
SCOPE-Lo
BFO
D52 MA862
IC9 LA1145M
Q32 DTC144
Q33
Q87 2SC4211
IC14 BU4066BCFV-E1
IC14A
IC14B
IC14C
IC14D
Q56 2SC4211
Q34 XP4601
Q37 2SC4211
Q38 XP4311
Q35 2SK882
Q36 DTC144EU
NB ON : 4.8 V
NB OFF: 0 V
SCAD
WFDT
AFE
AFO
NB
A
B
C
D



IC5 μPC2721GV
Q85 2SC4211
FI2 SFE10.7MV
FI3 SFT10.7MS2-A
D46 MA862
D47 MA862
D49 MA862
D50 MA862
Q39 3SK131
Q40 2SC4211
Q41 2SK882
L108 LS-513
Q77 2SC4835 R
Q76 2SC5193
IC23 μPB1509GV
Q86 2SK882
X1 CR-588 (10.25 MHz)
D56 1SV230
FI5 CFWS450K3
FI6 CFWS450HT
FI7 CFWS450E
D57 MA862
D58 MA862
D59 MA862
D60 MA862
D61 DAN222
Q44 DTC144EU
Q31 XP4311
IC8 TA31136FN
FI4 CFWS450HT
IC9 LA1145M
Q32 DTC144EU
Q33 2SC4211
Q35 2SK882
L106 LS-513
L107 LS-513
D53 1SS375
Q37 2SC4211
Q38 XP4311
Q48 2SK882
Q49 2SC4211
L112 LS-510
D63 1SS375
Q51 2SC4211
IC12 μPC1037GR-E1
REFV
FIL0
FIL1
FIL2
FIL3
FIL4
FIL5
SCAD
AFWF
AGC
/WF5
BFO
BW 15 kHz 4.3 V 50 kHz
CMAD
AM SSB FM 4.5 V
AM SSB FM 0 V
NB ON : 0.38 V
NB OFF : 4.7 V
50 kHz: 4.0 V 230 kHz: 1.6 V
50 kHz: 4.8 V 230 kHz: 1.1 V
50 kHz: 1.1 V 230 kHz: 4.8 V
2.8 kHz: 2.7 V
5 kHz: 2.7 V
15 kHz: 2.7 V
50 kHz: 2.5 V
50 kHz: 2.4 V
A
B
C
D


Q39 3SK131
Q40 2SC4211
Q41 2SK882
L108 LS-513
D54 MA862
D55 MA862
WFM5
Q42 2SC4835-R
Q43 2SC4211-6
IC10 TA31136
IC27 TC4S66F
X1 CR-588 (10.25 MHz)
X2 CDBCA450CX24
D58 1SV230
Q44 DTC144EU
IC11A NJM2904M
IC11B NJM2904V
Q45 XP4601
D60 MA862
D61 DAN222
CTAD
CMAD
NOIS
AFFM
FDET
Q52 2SA1622
Q53 2SA1622-6
Q54 XP1213
AGC ON: 0 V, AGC OFF: 4.8 V
AGCF
SCAN
Q51 2SC4211
Q49 2SC4211
L112 LS-510
D63 1SS375
D64 1SS355
D65 1SS355
D66 1SS355
IC12 μPC1037GR-E1
IC13A NJM2904V
IC13B NJM2904V
Q89 2SC4211-6
Q88 DTC144EU
AFAM
SMAD
AGC
AFSB
B4B7