


BENISON

V9

VHF FM TRANSCEIVERS

Service Manual

INTRODUCTION

This service manual describes the latest service information for the **V9** at the time of publication.

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the transceiver to an AC outlet or to a DC power supply that uses more than 10.3 V. Such a connection could cause a fire hazard and/or electric shock.

DO NOT expose the transceiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the transceiver.

DO NOT apply an RF signal of more than 20 dBm (100mW) to the antenna connector. This could damage the transceiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

0910053802	PCB B-5649B	V9	MAIN UNIT	1 pieces
8810009560	Screw BT M2 x 6 ZK	V9	Chassis	10 pieces
8810009510	Screw BT 2 x 4 NI	V9	Chassis	10 pieces

Addresses are provided on the inside back cover for your convenience.



REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 40 dB to 50 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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SECTION 1 SPECIFICATIONS

■ GENERAL

• Frequency coverage	:	<table border="1"> <thead> <tr> <th>Version</th><th>Receive</th><th>Transmit</th></tr> </thead> <tbody> <tr> <td>[USA]</td><td rowspan="2">144.0000–146.9875 MHz*</td><td>144.0000–146.9875 MHz</td></tr> <tr> <td>[GEN]</td><td>144.0000–146.9875 MHz*</td></tr> </tbody> </table>	Version	Receive	Transmit	[USA]	144.0000–146.9875 MHz*	144.0000–146.9875 MHz	[GEN]	144.0000–146.9875 MHz*							
Version	Receive	Transmit															
[USA]	144.0000–146.9875 MHz*	144.0000–146.9875 MHz															
[GEN]		144.0000–146.9875 MHz*															
		*Specifications Guaranteed: 144.0000–146.9875 MHz only															
• Type of emission	:	F2D/ F3E															
• Frequency stability (–10°C to +60°C; +14°F to +140°F)	:	± 10 ppm															
• Tuning steps	:	5, 10, 12.5, 15, 20, 25, 30 or 50 kHz															
• Antenna connector	:	BNC (50) Ω															
• Power supply requirement (negative ground)	:	7.2 V DC (Operable voltage range: 6.0 to 10.3 V)															
• Number of memory channel	:	100 channels															
• Call channel	:	1 channel															
• Scanning mode	:	Program, Memory, Skip, Priority or Tone															
• Current drain (approx.)	:	<table> <tr> <td>Transmit</td><td>at High (5 W)</td><td>1.7 A</td></tr> <tr> <td></td><td>at Low (1 W)</td><td>0.7 A</td></tr> <tr> <td>Receive</td><td>Max. audio</td><td>250 mA</td></tr> <tr> <td></td><td>stand-by</td><td>70 mA</td></tr> <tr> <td></td><td>power saved</td><td>20 mA</td></tr> </table>	Transmit	at High (5 W)	1.7 A		at Low (1 W)	0.7 A	Receive	Max. audio	250 mA		stand-by	70 mA		power saved	20 mA
Transmit	at High (5 W)	1.7 A															
	at Low (1 W)	0.7 A															
Receive	Max. audio	250 mA															
	stand-by	70 mA															
	power saved	20 mA															
• Usable temperature range	:	–10°C to +60°C; +14°F to +140°F															
• Dimensions (projections not included)	:	54(W) × 132(H) × 35(D) mm; 2 1/8(W) × 5 3/16(H) × 1 3/8(D) in.															
• Weight (with ant., BP-222)	:	350 g; 12.3 oz.															

■ TRANSMITTER

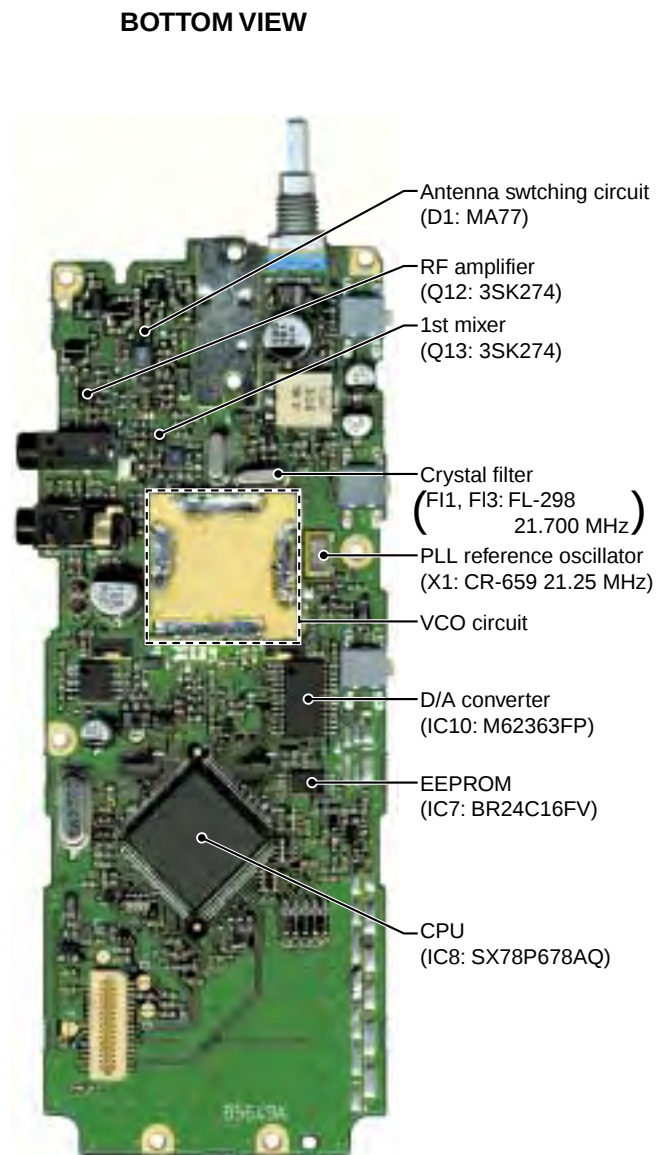
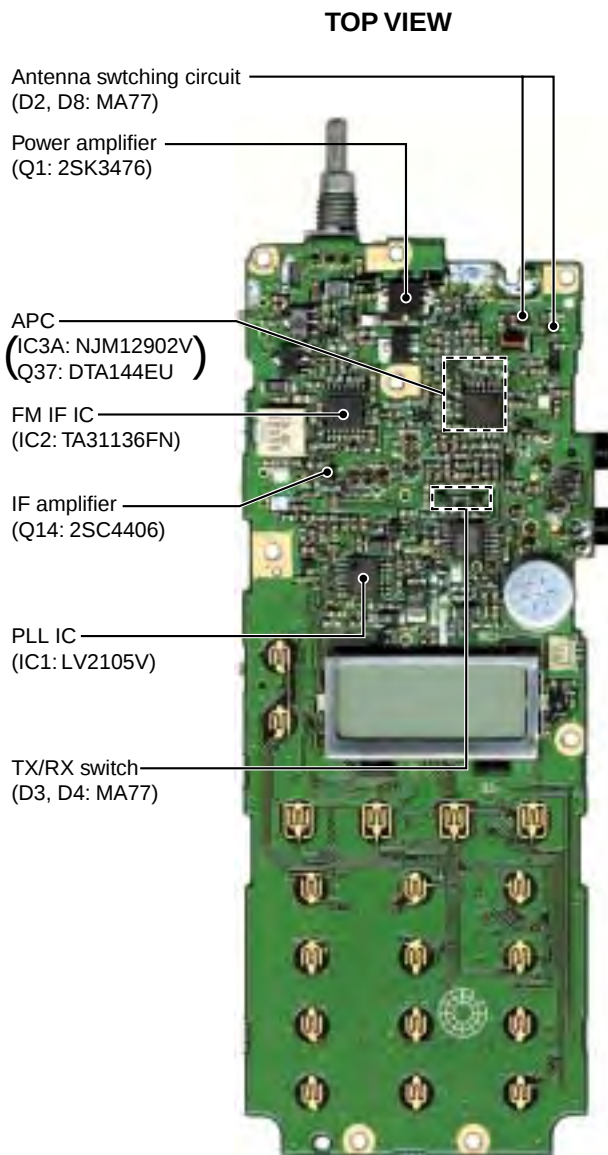
• RF output power (at 7.2 V DC) (with supplied battery pack)	:	5W / 1 W (High / Low)
• Modulation system	:	Variable reactance frequency modulation
• Maximum frequency deviation	:	±2.5 kHz
• Spurious emissions	:	Less than –60 dB
• Ext. microphone connector	:	3-conductor 2.5(d) mm (1/10")/2.2 kΩ

■ RECEIVER

• Receive system	:	Double conversion superheterodyne system
• Intermediate frequencies	:	1st 38.85 MHz 2nd 450 kHz
• Sensitivity	:	0.16 μV at 12 dB SINAD (typical)
• Squelch sensitivity	:	0.1 μV at threshold (typical)
• Adjacent channel selectivity	:	65 dB (typical)
• Spurious response rejection	:	75 dB (typical)
• Intermodulation rejection ratio	:	65 dB (typical)
• Audio output power (at 7.2 V DC)	:	More than 300 mW at 10% distortion with an 8 Ω load
• Ext. speaker connector	:	3-conductor 3.5(d) mm (1/8")/8 Ω

All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEWS

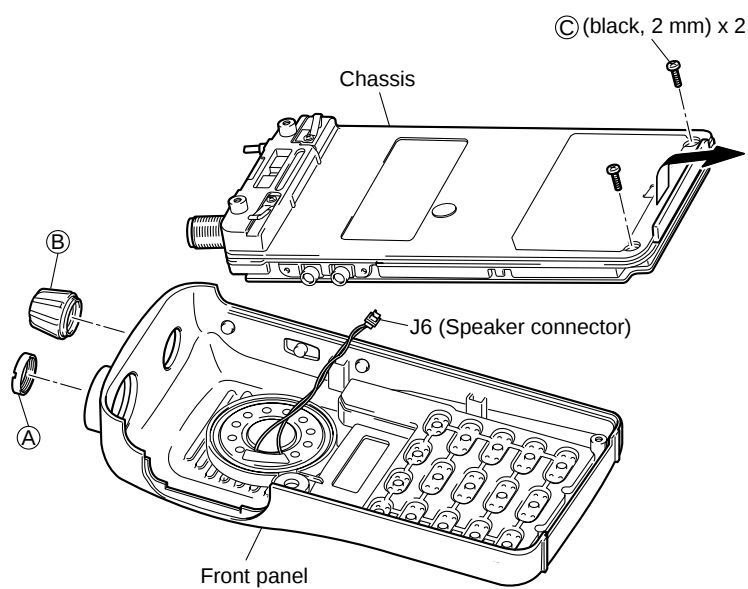


SECTION 3 DISASSEMBLY INSTRUCTIONS

3-1 DISASSEMBLY INSTRUCTION

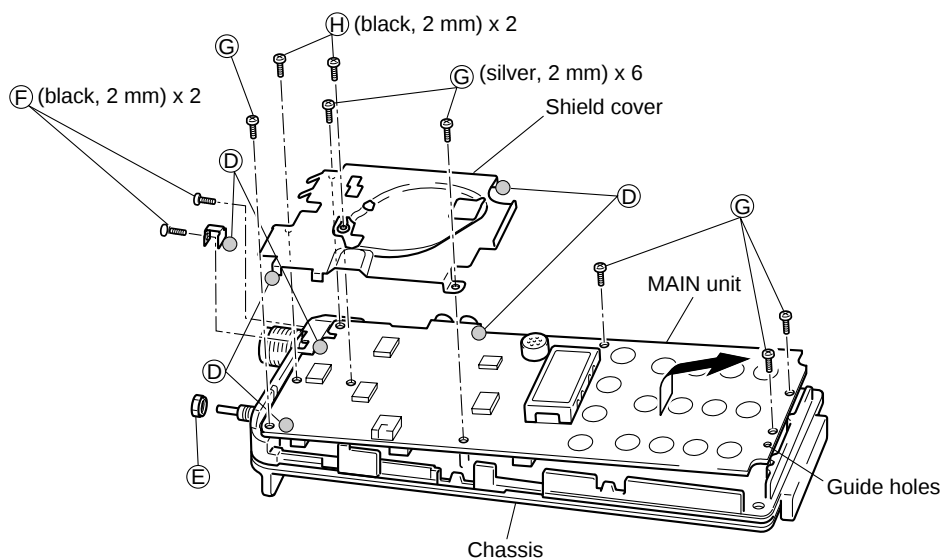
• REMOVING THE CHASSIS PANEL

- ① Unscrew 1 nut (A), and remove 1 knob (B).
- ② Unscrew 2 screws (C).
- ③ Take off the chassis in the direction of the arrow.
- ④ Unplug J6 to separate front panel and chassis.



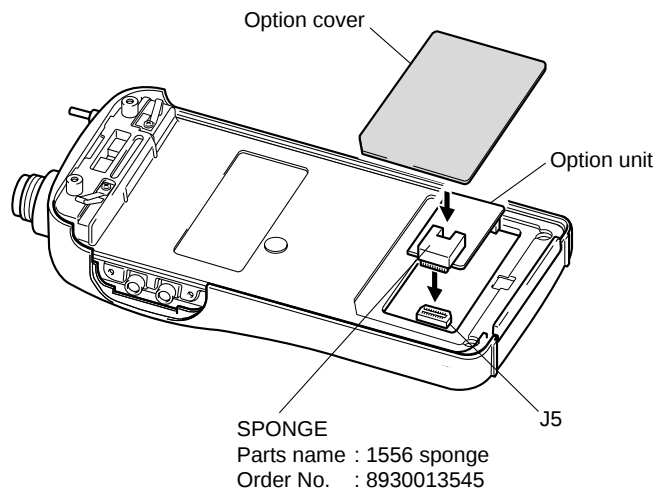
• REMOVING THE MAIN UNIT

- ① Unsolder 3 points (D), and unscrew 1 nut (E).
- ② Unscrew 2 screws (F), 2 screws (H), and 6 screws (G) (silver, 2 mm) to separate the chassis and the MAIN unit.
- ③ Take off the MAIN unit in the direction of the arrow.



3-2 OPTIONAL UNIT INSTALLATIONS

- ① Remove the option cover.
- ② Remove the bottom protective paper of spoge.
- ③ Connect the UT-108 optional unit to J5.
- ④ Replace the option cover to the chassis-hole.



SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT

Received signals passed through the low-pass filter (L1, L2, C1–C5). The filtered signals are applied to the $1/4 \lambda$ type antenna switching circuit (D1, D2, D8, L15, C76).

The antenna switching circuit functions as a low-pass filter while transmitting. However, its impedance becomes very high while D2 and D8 are turn ON. Thus transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a $1/4 \lambda$ type diode switching system. The passed signals are then applied to the RF amplifier circuit.

4-1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit are applied to the limiter (D50), and are then passed through the band-pass filter (D9, L16, C80). The filtered signals are amplified at the RF amplifier (Q12), then applied to the 1st mixer circuit after out-of-band signals are suppressed at the band-pass filter (D11, D12, L19, C91–C97).

D9, D11, D12 employ varactor diodes that track the band-pass filters and are controlled by the T1–T3 signals from the D/A convertor (IC10, pins 2, 3, 10). These diodes tune the center frequency of an RF passband for wide bandwidth receiving and good image rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will pass through two crystal filters at the next stage of the 1st mixer.

The signals from the RF circuit are mixed at the 1st mixer (Q13) with a 1st LO signal coming from the VCO circuit to produce a 21.70 MHz 1st IF signal.

The 1st IF signal is applied to two crystal filters (FI1 and FI3) to suppress out-of-band signals. The filtered 1st IF signal is applied to the IF amplifier (Q14), then applied to the 2nd mixer circuit (IC1, pin 16).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double conversion superheterodyne system (which converts receive signal twice) improves the image rejection ratio and obtain stable receiver gain.

The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC2, pin 16), and is mixed with the 2nd LO signal to be converted to a 450 kHz 2nd IF signal.

The FM IF IC contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 21.25 MHz 2nd LO signal is produced at the PLL circuit.

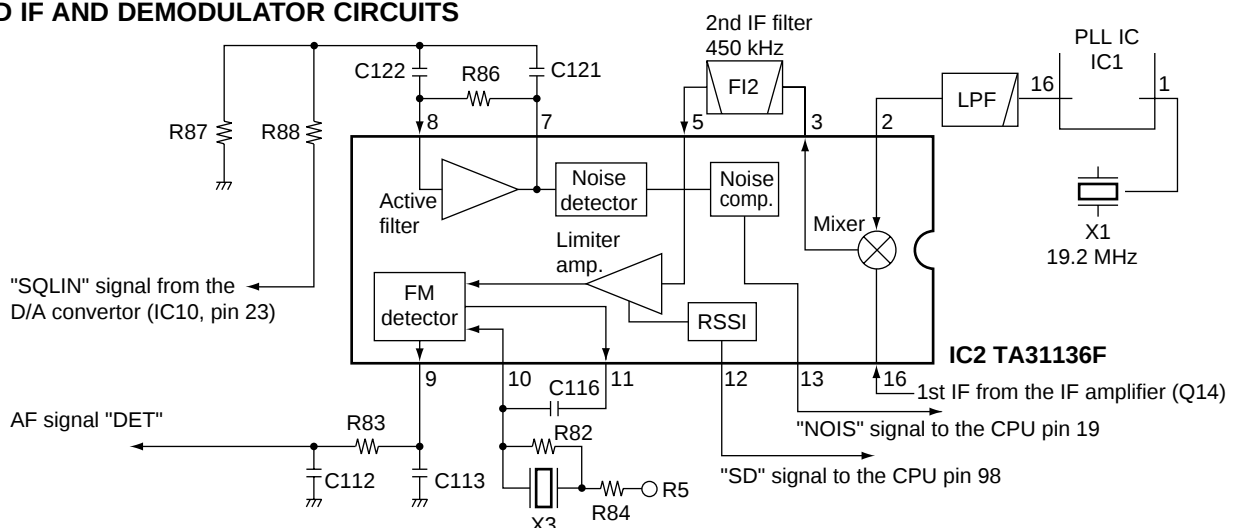
The 2nd IF signal from the 2nd mixer (IC2, pin 3) passes through a ceramic filter (FI2) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (IC2, pin 5) and applied to the quadrature detector (IC2, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

4-1-5 AF CIRCUIT

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

AF signals from the FM IF IC (IC2, pin 9) are applied to the analog switch (IC4, pin 1) via the AF filter circuit (IC3b, pins 6, 7). The output signals from pin 2, 3 are passed through the low-pass filter (IC3d, pins 13, 14), and are then applied to the analog switch (IC4, pin 9, 10) again. The signals from the IC4, pin 11 are applied to the AF power amplifier (IC5, pin 4) after passing through the D/A convertor (IC10, pins 12, 11).

• 2ND IF AND DEMODULATOR CIRCUITS



The AF signals are applied to the AF power amplifier circuit (IC5, pin 4) to obtain the specified audio level. The amplified AF signals, output from pin 10, are applied to the internal speaker (SP1) via the speaker jack (CHASSIS unit; J3) when no plug is connected to the jack.

4-1-6 SQUELCH CIRCUIT

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch switches the analog switch.

A portion of the AF signals from the FM IF IC (IC2, pin 9) are applied to the active filter section (IC2, pin 8) where noise components are amplified and detected with an internal noise detector.

The trigger circuit converts the detected signals to a HIGH or LOW signal and applies this (from pin 13) to the CPU (IC8, pin 19) as the NOIS signal. When the CPU receives a HIGH level NOIS signal, the CPU controls the RMUT line to cut the AF signals at the analog switch IC (IC4). At the same time, the AFON line controls the AF regulator circuit (Q15, Q16) to cut out the VCC power source for the AF power amplifier (IC5).

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals with +6 dB/octave pre-emphasis from the microphone to a level needed for the modulation circuit.

The AF signals from the microphone are applied to the microphone amplifier circuit (IC3c, pin 10). The amplified AF signals are passed through the low-pass filter circuit (IC3d, pins 13, 14) via the analog switch (IC4, pins 4, 3). The filtered AF signals are applied to the modulator circuit after passing through the analog switch (IC4, pins 8, 9).

4-2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The audio signals (SHIFT) change the reactance of D37 to modulate an oscillated signal at the VCO (Q50, D38). The oscillated signal is amplified at the LO (Q6) and buffer (Q4) amplifiers, then applied to the TX/RX switch circuit (D3, D4).

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS

The signal from the VCO circuit passes through the TX/RX switching circuit (D3) and is amplified at the pre-drive (Q3), drive (Q2) and power (Q1) amplifiers to obtain 5.5 W of RF power (at 7.2 V DC/typical). The amplified signal passes through the low-pass filter (L4, C278, C287), and then applied to the antenna switching circuit (D1). The signal is applied to the antenna connector (J1) after being passed through the low-pass filter (L1, L2, C1–C5).

The bias current of the drive (Q2) and power (Q1) amplifiers is controlled by the APC circuit to stabilize the output power.

4-2-4 APC CIRCUIT

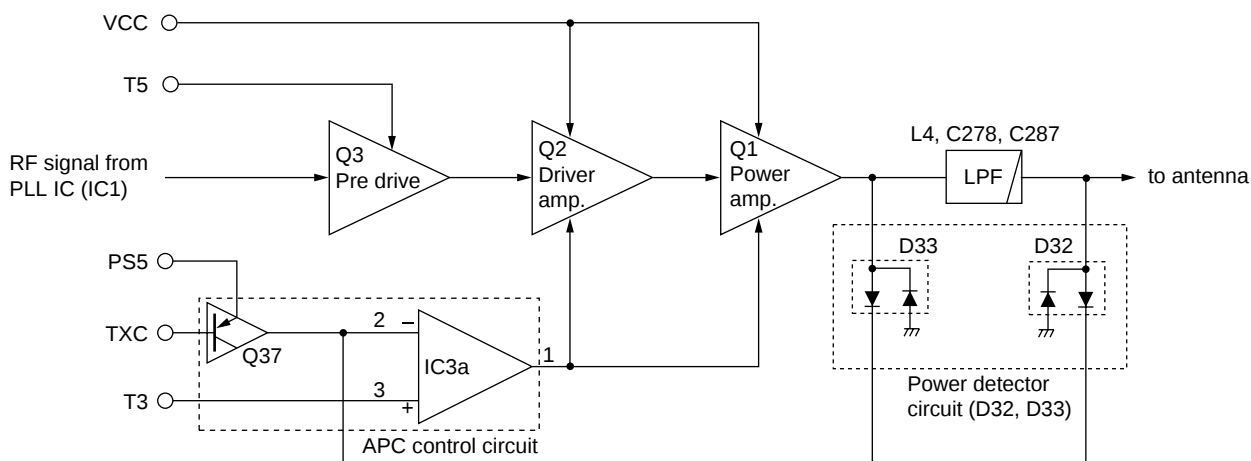
The APC (Automatic Power Control) circuit (IC3a, Q37) protects drive and power amplifiers from excessive currents and selects HIGH or LOW output power.

The output voltage from the power detector circuit (D32, D33) is applied to the differential amplifier (IC3a, pin 2), and the "T3" signal from the D/A convertor (IC10, pin 10) is applied to the other input for reference.

When the driving current increases, the input voltage of the differential amplifier (IC3a, pin 2) will be increased. In such cases, the differential amplifier output voltage (pin 1) is decreased to reduce the drive current.

Q37 is controlled by the TXC signal from the CPU (IC8, pin 55) to select HIGH or LOW output power.

• APC CIRCUIT



4-3 PLL CIRCUITS

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains the VCO circuit (Q50, D38). The oscillated signal is amplified at the LO (Q6) and buffer (Q5) amplifiers and then applied to the PLL IC (IC1, pin 6).

The PLL IC contains a prescaler, programmable counter, programmable divider, phase detector, charge pump, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

If the oscillated signal drifts, its phase changes from the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

A portion of the VCO circuit is amplified at the LO (Q6) and buffer (Q4) amplifiers and is then applied to the receive 1st mixer or transmit pre-drive amplifier circuit via the TX/RX switching diode (D3, D4).

4-4 OTHER CIRCUITS

4-4-1 TONE SQUELCH CIRCUIT

A portion of the detected audio signals from the "DET" line are passed through the tone filter (Q53). The filtered signal is then applied to the CPU (IC1, pin 94) via the "CTCIN" signal, and is compared with the programmed tone signal. The CPU (IC1) outputs control signals as "CTCC" signal to the AF mute and AF regulator circuits to open the squelch when a matched tone signal is received.

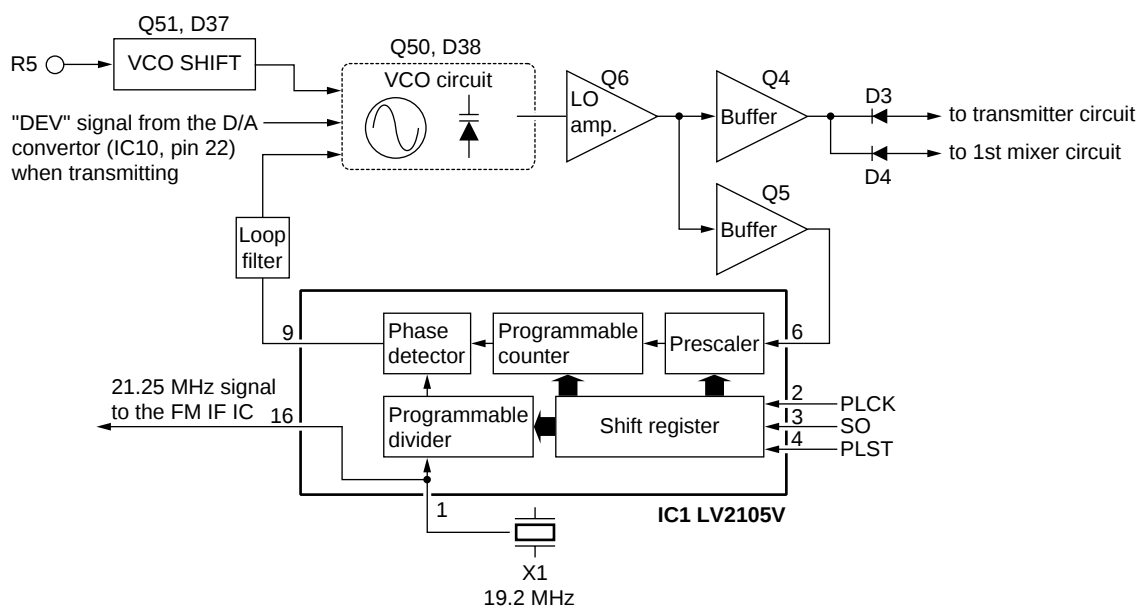
The programmed subaudible tone signal is output from the CPU (IC1, pin 91) directly when transmitting with a tone.

4-5 POWER SUPPLY CIRCUITS

VOLTAGE LINE

LINE	DESCRIPTION
VCC	The voltage from the attached battery pack.
CPU5	Common 5 V converted from the VCC line by the CPU5 regulator (IC12). The output voltage is applied to the CPU (IC8), EEPROM (IC7) and reset IC (IC11).
SW5V	Common 5 V converted from the VCC line by the SW5 regulator circuit (Q55, Q57, D39). The output voltage is applied to the T5, R5, PS5 and VCO5 regulator circuits, D/A convertor (IC10, pin 16), etc.
VCO5	Common 5 V converted from the SW5V line by the VCO5 regulator circuit (Q11) using the LO (Q6) and buffer (Q4, Q5) amplifiers. The VCO5 regulator circuit is controlled by the PSVCO line from the CPU (IC8, pin 62).
PS5	Common 5 V converted from the SW5V line by the PS5 regulator circuit (Q54) using the analog switch (IC14, pin 14) and APC controller (Q37). The PS5 regulator circuit is controlled by the PS5C line from the CPU (IC8, pin 63).
R5	5 V for receiver circuits converted from the SW5V line by the R5 regulator circuit (Q21) using the 2nd IF IC (IC2, pin 4), RF (Q12) and IF (Q14) amplifiers, etc. The R5 regulator circuit is controlled by the R5C line from the CPU (IC8, pin 53).
T5	5 V for the transmitter circuit converted from the SW5V line by the T5 regulator circuit (Q22) using the pre-drive amplifier (Q3). The T5 regulator circuit is controlled by the T5C line from the CPU (IC8, pin 54).

• PLL CIRCUIT



4-6-2 D/A CONVERTOR IC (IC10)

Pin number	Port name	Description
2, 3	T1, T2	Output tunable bandpass filter control signals.
10	T3	• Outputs tunable bandpass filter control signal while receiving. • Outputs TX power control signal while transmitting.
11	VOLOUT	Outputs AF volume control signal.
14	DTC	Outputs DTCS's gradient control signal.
15	FC	Outputs reference frequency control signal to X1.
22	DEV	Outputs transmit deviation control signal.
23	SQLIN	Outputs squelch control signal.

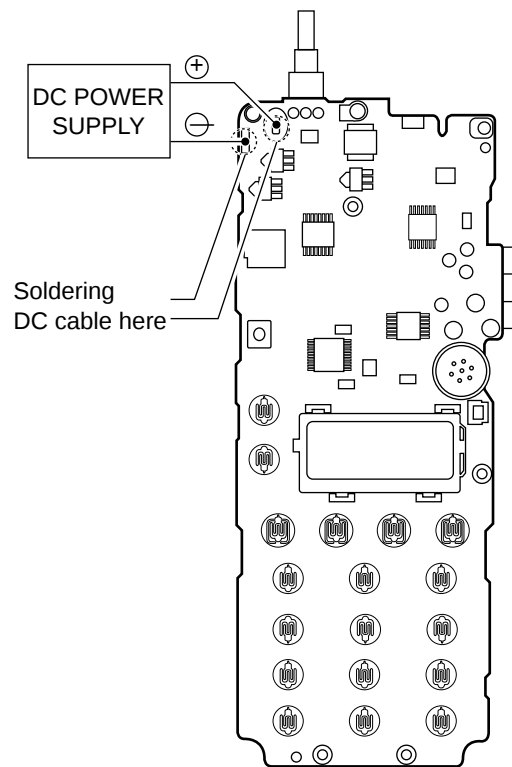
SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 7.2 V DC Current capacity : 5 A or more	Digital multimeter	Input impedance : 10 M Ω /V DC or better

• DC POWER CABLE CONNECTION



Top view

Designator	Comment	Designator	Comment
R105	1K	R250	100K
R106	47K	R251	100K
R111	3K3	R252	150K
R112	10K	R253	47R
R113	22R	R254	NC
R114	680R	R255	470R
R118	NC	R256	680K
R119	NC	R257	2K7
R120	NC	R266	180K
R121	NC	R267	3K3
R122	NC	R268	150K
R125	10R	R272	100K
R131	47K	R273	100K
R132	47R	R275	1K5
R133	47K	R277	10R
R141	47K	R282	4K7
R142	47K	R283	4K7
R143	47R	R284	4K7
R153	270R	R302	1K
R154	270R	R303	47K
R163	82K	R305	10K
R172	22K	R306	10K
R174	10K	R307	10K
R175	2K2	R317	0R
R176	10K	R318	150R
R177	100K	R319	47K
R178	56K	R320	560R
R181	180K	R321	560R
R182	330K	R322	6K8
R205	1K	R323	2K2
R216	100K	R324	0R
R221	100K	R325	22K
R222	100K	R326	100K
R223	220K	R327	100K
R224	100K	R329	0R
R225	47R	R342	100R
R227	100R	R345	1K
R232	100K	R346	100R
R236	100K	R348	100R
R237	100K	R357	150R
R241	0R	R361	4K7
R242	10K	R370	100R
R244	1K	R371	120K
R247	470R	R373	3K3
R248	100R	R374	100R
R249	150K	R375	1K

Designator	Comment	Designator	Comment
R376	5K6	R537	10K
R377	47R	R538	1K5
R378	3K3	R539	100K
R380	15K	R540	18K
R401	22K	R541	1M
R403	2K2	R542	120K
R411	100K	R543	39K
R412	100R	R547	470R
R413	100R	R549	0R
R414	15K	R711	4K7
R415	100K	R728	47K
R416	680R	R811	1K
R417	100K	R812	10K
R418	10K	R813	1K
R419	22K	R814	220R
R421	15K	R815	4K7
R425	NC	R816	220K
R474	10K	R817	10K
R476	2K2	R818	1K
R477	10K	R819	1K
R480	10K	R822	15K
R481	22K	R823	82K
R482	150R	R824	100K
R483	10R	R826	1K
R484	0R	R827	1K
R488	15K	R828	47K
R491	4K7	R829	47K
R492	150K	R830	10K
R493	0R	R841	470K
R494	1M	R842	120K
R517	150K	R843	47K
R518	10K	R901	0R
R519	10K	C101	104P
R520	10K	C102	NC
R521	NC	C105	470P
R522	10K	C106	103P
R523	NC	C107	104P
R525	10K	C111	20P
R526	100K	C114	470P
R528	NC	C118	10P
R529	NC	C120	NC
R530	82K	C122	NC
R532	220K	C125	15P
R533	33K	C126	470P
R534	18K	C127	NC
R536	120K	C133	102P

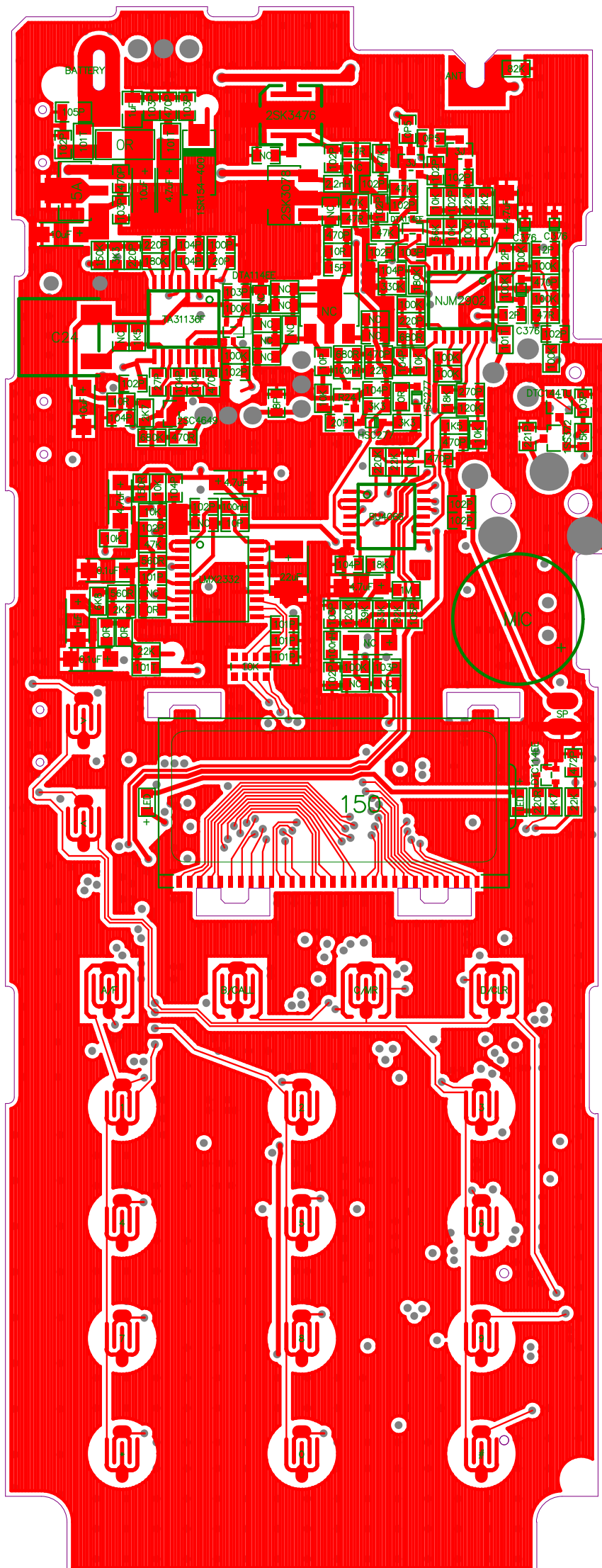
Designator	Comment	Designator	Comment
C134	103P	C224	470P
C135	470P	C225	470P
C136	NC	C227	470P
C137	102P	C228	12P
C142	102P	C229	2P
C143	NC	C230	4P
C144	470P	C231	12P
C145	103P	C234	2P
C146	27P	C235	12P
C147	NC	C237	102P
C149	3T	C238	5P
C150	NC	C240	470P
C152	68P	C242	470P
C153	470P	C244	10P
C154	470P	C245	6P
C155	15P	C246	10P
C156	470P	C248	103P
C157	20P	C250	470P
C158	12P	C251	102P
C159	20P	C252	103P
C160	15P	C253	104P
C161	20P	C255	8P
C162	12P	C257	104P
C163	NC	C260	470P
C171	0P5	C261	20P
C172	102P	C262	100P
C173	0P5	C263	104P
C174	102P	C264	104P
C175	102P	C265	104P
C176	102P	C266	220P
C177	104P	C267	220P
C178	103P	C271	104P
C179	102P	C272	102P
C182	104P	C273	104P
C201	103P	C275	27P
C205	470P	C276	104P
C206	103P	C277	103P
C207	103P	C278	NC
C211	6P	C281	102P
C212	10P	C282	473P
C214	4P	C284	103P
C215	1P	C301	104P
C216	12P	C302	470P
C218	0R	C303	103P
C220	470P	C304	103P
C223	470P	C310	100P

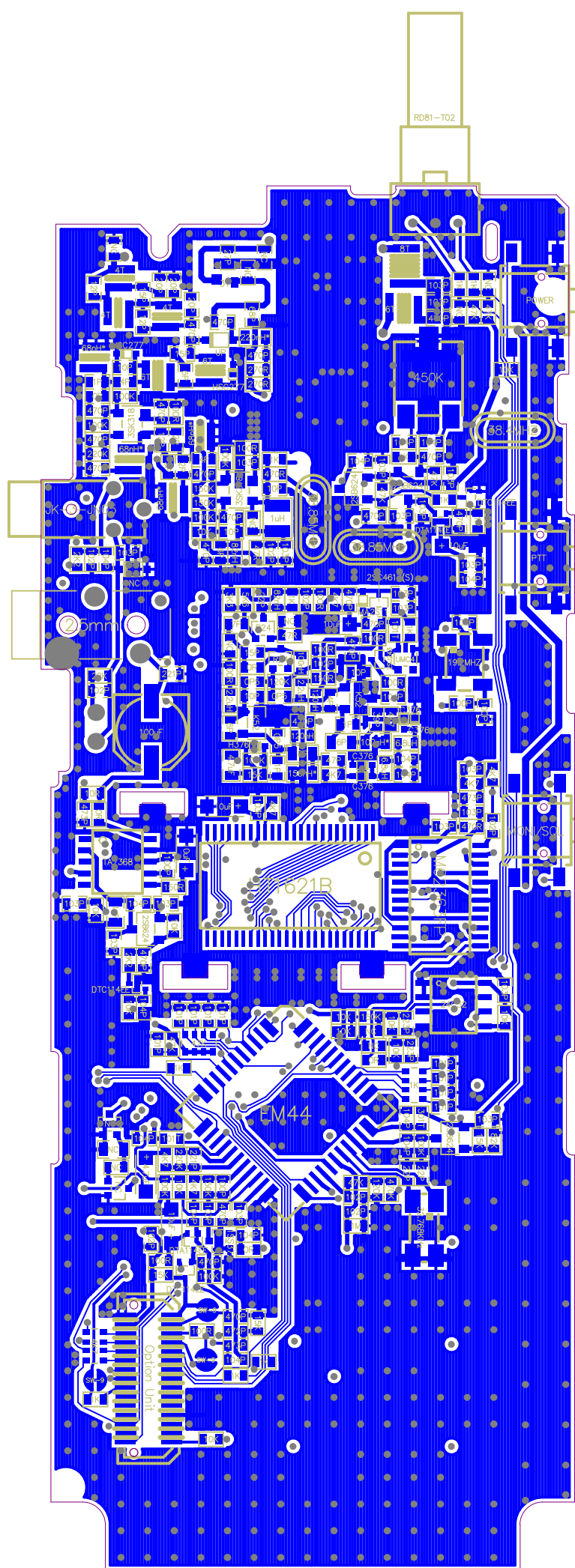
Designator	Comment	Designator	Comment
C311	101P	C415	472P
C312	101P	C416	104P
C313	101P	C417	220P
C314	100P	C421	470P
C315	102P	C425	NC
C316	NC	C473	103P
C317	101P	C474	104P
C318	104P	C475	103P
C319	102P	C476	470P
C327	102P	C477	104P
C328	NC	C480	103P
C329	10P	C481	472P
C331	104P	C482	100P
C332	47P	C483	473P
C333	1P	C484	221P
C338	150nH*	C485	102P
C340	6P	C486	102P
C341	0P5	C488	103P
C342	10P	C489	221P
C343	0P5	C491	104P
C347	470P	C492	100P
C348	104P	C493	104P
C349	470P	C494	102P
C350	104P	C495	103P
C351	39P	C521	223P
C352	100nH*	C523	223P
C355	4P	C525	470P
C356	1P	C531	470P
C357	10P	C533	103P
C358	0P5	C536	270P
C361	103P	C538	470P
C362	470P	C542	103P
C363	470P	C544	105P
C371	102P	C545	104P
C372	15P	C547	103P
C373	7P	C548	102P
C375	102P	C549	103P
C377	NC	C711	103P
C378	22P	C721	101P
C401	102P	C722	101P
C402	103P	C723	101P
C403	102P	C724	101P
C404	104P	C725	101P
C411	470P	C726	101P
C413	104P	C727	101P
C414	473P	C728	101P

Designator	Comment	Designator	Comment
C729	101P	D902	1SR154-400
C811	104P	E144	1uF
C812	103P	E145	4. 7uF
C813	102P	E179	4. 7uF
C816	221P	E201	10uF
C821	104P	E277	10uF
C822	103P	E283	4. 7uF
C824	104P	E301	4. 7uF
C825	22P	E305	4. 7uF
C826	22P	E315	22uF
C828	NC	E321	0. 1uF
C829	NC	E322	1uF
C830	103P	E324	0. 1uF
C843	102P	E362	10uF
C901	105P	E380	4. 7uF
C902	102P	E412	10uF
C903	103P	E425	NC
C908	103P	E475	1uF
C909	470P	E482	10uF
C910	103P	E484	100uF
CR261	38. 4MHZ	E529	NC
CR275	C24	E539	4. 7uF
CR318	19. 2MHZ	E711	10uF
CR825	32. 768KHz	E908	10uF
D111	HSC277	E910	10uF
D154	UP	FL254	38. 85MHz
D171	3J	FL255	38. 85MHz
D173	3J	FL263	450K
D211	HSC277	JK401	JK-3-JN05
D212	HSC277	JK485	2. 5mm
D216	C376	JP811	Option Unit
D231	C376	L114	100nH
D235	C376	L122	NC
D241	HSC277	L135	6T
D331	C376	L136	2. 2nH
D332	C376	L144	101T
D333	H376	L145	8T
D350	C376	L154	220nH*
D351	C376	L158	4T
D361	MA2S11	L160	4T
D402	NC	L162	4T
D425	NC	L211	6T
D489	1SS372	L212	6T
D493	1SS372	L215	68nH*
D813	LED	L225	68nH*
D814	LED	L230	68nH*

Designator	Comment	Designator	Comment
L238	68nH*	S732	1
L245	82nH	S733	4
L254	1uH	S734	7
L315	100nH	S735	*
L324	0R	SP485	SP
L325	101T	SW400	POWER
L326	100nH	SW401	PTT
L331	6. 8uH	SW411	SW-9
L332	4K7	SW413	SW-9
L339	8P	SW813	SW-9
L342	2. 2uH	SW826	RD81-T02
L347	120nH	T105	DTC114EE
L348	120nH	T106	2SB624
L350	6. 8uH	T112	R24
L351	4K7	T120	NC
L353	6P	T133	2SK3078
L357	2. 2uH	T145	2SK3476
L363	101T	T178	DTA114EE
L371	100nH	T206	DTA114EE
L372	NC	T226	3SK318
L375	82nH	T248	3SK318
L401	101T	T255	2SC4649
L811	101T	T272	DTA114EE
L821	301T	T302	2SB624
L901	101T	T340	K52
LCD711	V9 150	T344	UMC4
MIC401	MIC	T348	2SJ243
PR311	10K	T355	K52
PR727	1K	T362	2SC4617 (S)
PR728	47K	T371	R24
RP813	4K7	T377	R24
S701	<	T412	DTA114EE
S702	A/F	T421	DTC114EE
S703	B/CALL	T425	NC
S704	C/MR	T474	2SB624
S705	D/CLR	T476	DTC114EE
S711	>	T488	DTC144TU
S712	3	T814	DTC114EE
S713	6	T822	2SB624
S714	9	U261	TA31136F
S715	#	U311	LMX2332
S721	MONI/SQL	U481	TA7368
S722	2	U511	NJM2902
S723	5	U544	BU4066
S724	8	U547	M62363FP
S725	0	U711	HT1621B

[illegible]





SECTION 10 BC-146 OPTIONAL DESKTOP CHARGER INFORMATION

10-1 PARTS LIST

[CHARGE UNIT]

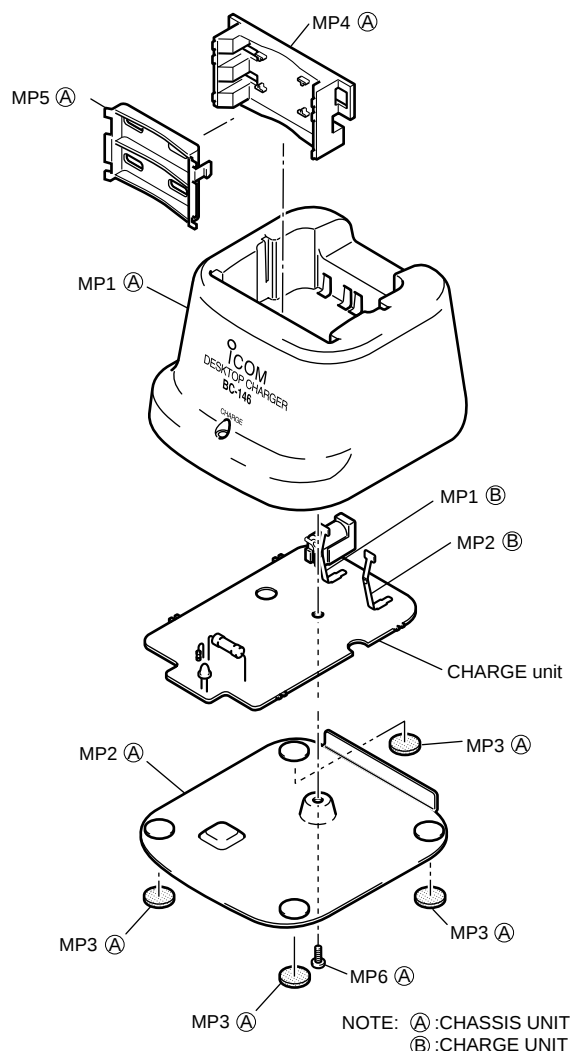
REF. NO.	ODER NO.	DESCRIPTION	QTY.
R1	7010007550	RESISTOR ERG3SJ680H	1
R2	7010007100	RESISTOR PSD1/4V 1 kΩ	1
J1	6510021470	CONNECTOR HEC0470-01-230	1
DS1	5040001390	LED TLG124A	1
EP1	0910053820	PCB B 5650	1
MP1	8930051340	2338 TERMINAL	1
MP2	8930051340	2338 TERMINAL	1

[CHASSIS UNIT]

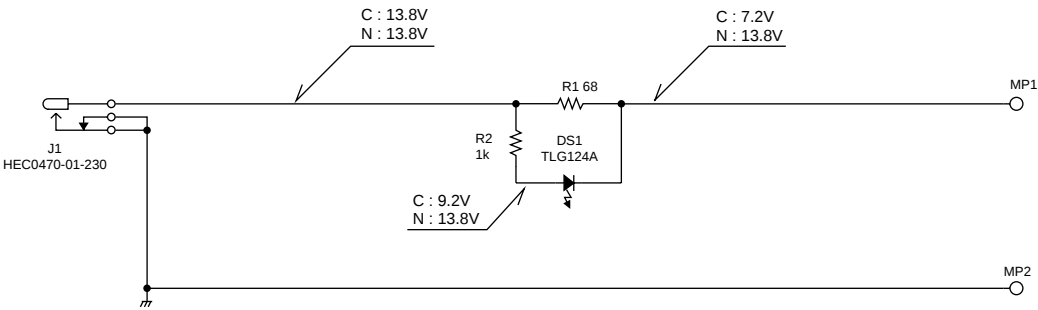
REF. NO.	ODER NO.	DESCRIPTION	QTY.
MP1	8010018620	2447 case (A)	1
MP2	8110007450	2447 cover	1
MP3	8930039620	Leg cushion (A)	4
MP4	8930055020	2480 spacer	1
MP5	8930055030	2480 BC-spacer	1
MP6	8810008660	Screw B0 M 3 x 8 NI-ZU (BT)	1

Screw abbreviations B0, BT:Self-tapping
NI-ZU :Nickel-Zinc

10-2 DISASSEMBLY INFORMATION



10-3 VOLTAGE DIAGRAM



10-4 BOARD LAYOUT

